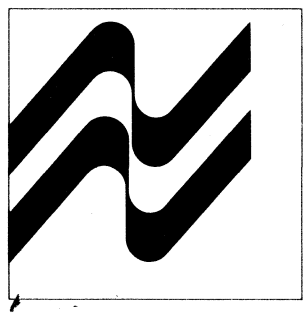
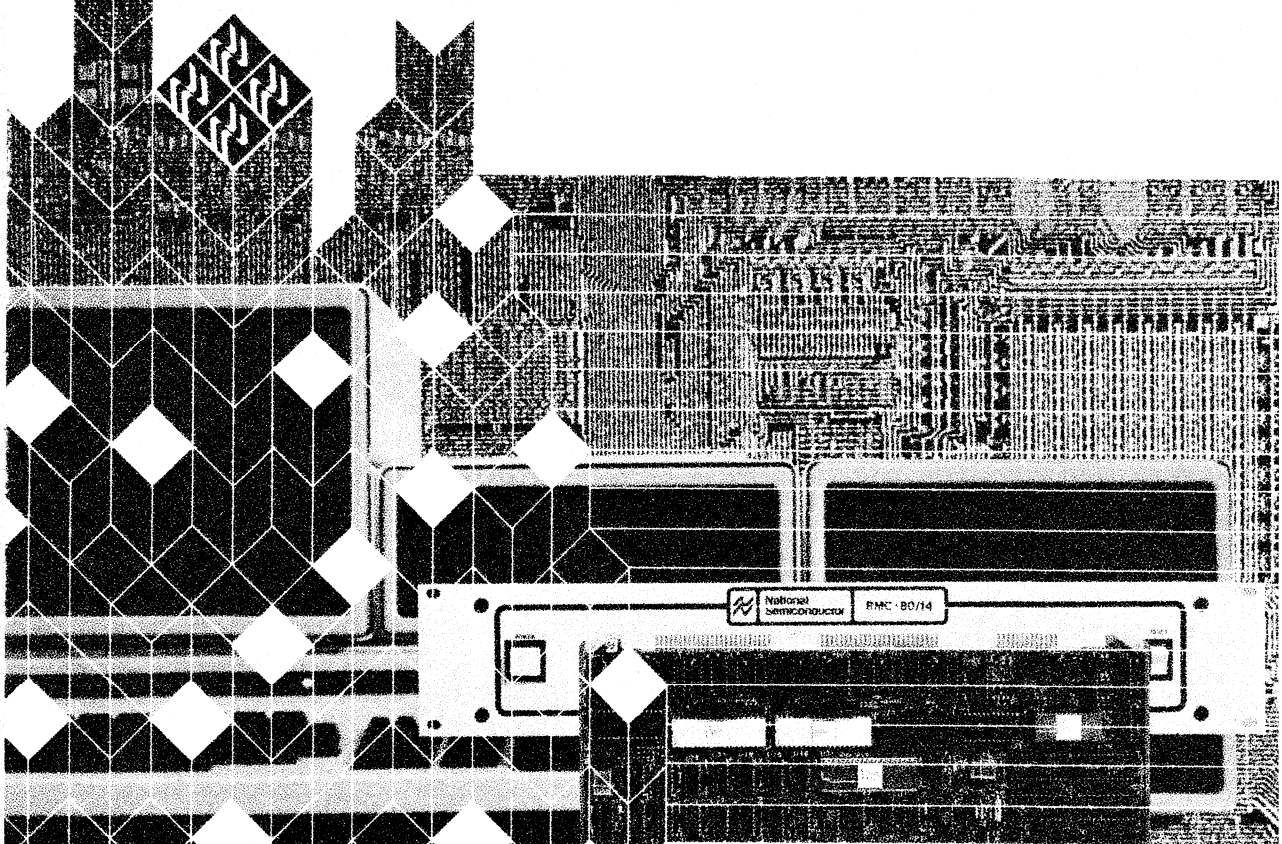
SERIES/80
BOARD LEVEL COMPUTER
STARPLEX
DEVELOPMENT SYSTEM
DATABOOK

NATIONAL
SEMICONDUCTOR



National Semiconductor Microcomputer Systems Series/80 Databook



January 1980

The National Series/80 Family

Introduction

The Series/80 product family from National Semiconductor provides a comprehensive base of Microcomputer Products. Fully compatible with the industry standard Series/80 architecture, many of these products are plug-for-plug, second source replacements for existing Intel* SBC products.

As well as being completely compatible with SBC products, National Series/80 products offer significant improvements such as greater reliability, more convenient user options, cleaner design and a full one year warranty. This saves the user design implementation time, lowers the cost of ownership and reduces inventory requirements.

Beyond providing a source for improved industry standard products, National's Series/80 family features proprietary products of totally new and differentiated design. As National's objective is to satisfy user demands, product engineers are allowed complete freedom to create new designs to meet the demands of the market. The STARPLEX™ Development System is one example of National's response to industry needs.

National's Series/80 family presently includes more than 80 individual computer products — everything needed to design advanced microcomputer systems.

This data book provides summary information on the complete line of board and system level microcomputer products, as well as information about the National Semiconductor STARPLEX Development System. The National Series/80 product line is based around a broad series of Board Level Microcomputers. Each of these microcomputers is a complete system containing CPU, read/write memory, sockets for read only memory, parallel and serial I/O and bus interface circuitry on a single printed circuit board. These same CPU boards are also integrated into rack mountable computer (RMC) systems providing low cost packaged systems that include a microcomputer, power supply, card cage, chassis and front panel. Single board microcomputers and packaged systems are complemented by a wide variety of system expansion products including RAM and ROM/PROM memory, parallel and serial I/O, analog I/O, DMA and peripheral controllers. All of the National Semiconductor Series/80 products are compatible with the Intel MULTIBUS™ bus structure.

The National Semiconductor STARPLEX Development System supports the development of National microcomputer and microprocessor based products. Designed with the user's needs in mind, all the facilities necessary for the development of hardware and software packages are integrated into the STARPLEX system. Single-keystroke controls are provided for the software package that includes operating system, text editor, debugger, link editor, loader, file manager, macro assembler, FORTRAN, BASIC and many utility packages.

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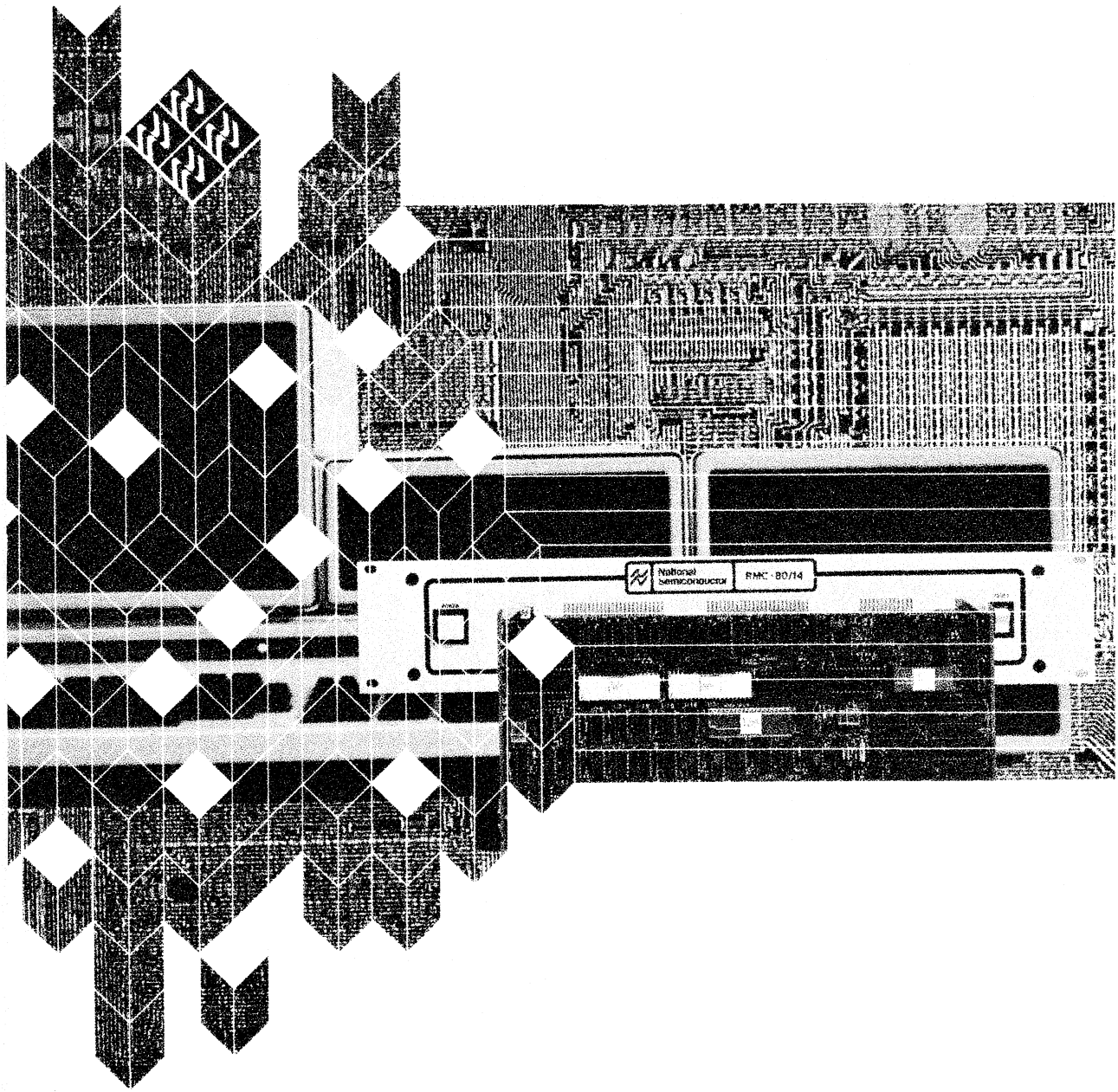
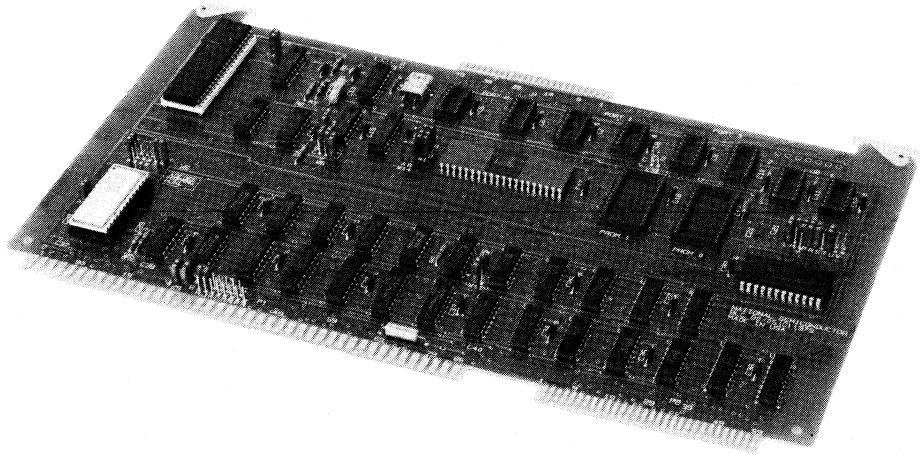
Section 1
Board Level Computers



National Semiconductor

BLC-80/05
Series/80 Board Level Computer



- **Complete System Capability, Including:**
  - 4 vectored interrupts
  - Multiple processor capability — up to six bus masters
  - 14-bit programmable timer
  - 512 bytes of static RAM — up to 8K bytes of EPROM/ROM
  - 22 programmable parallel I/O lines
  - TTL serial I/O interface
- **8085 CPU**
- **Single 5V Power Supply**
- **Compatible With Industry Standard BLC/SBC Series/80 Software and Hardware**
- **Plug-for-Plug Compatible With the Intel SBC-80/05**

Product Overview

The BLC-80/05 is a self-contained board level computer based on the 8085A CPU. Features on the BLC-80/05 allow building powerful and complex systems, particularly those requiring multi-processor configurations. This is provided by special bus arbitration logic incorporated on the board to sort out all contention disputes among processors sharing the same system bus.

Advanced features such as vectored interrupts and an on-board programmable timer greatly reduce the software generation effort for many applications. When combined with the computing power of the 8085A and the I/O capability of the 8085 chip set, the BLC-80/05 becomes an excellent candidate for a high performance, low cost, processor in a multi-processor system.

The BLC-80/05 is compatible with the large family of Series/80 products. This brings into feasibility the construction of systems with virtually limitless applications.

Functional Description

Central Processor

The powerful 8-bit 8085A is the central processor for the BLC-80/05. It is directly software compatible with the popular 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds.

Memory

- 512 bytes are provided by the 8155 RAM/IO/TIMER and two MM2111As.
- Sockets on-board for 2K, 4K, or 8K bytes of EPROM/ROM using MM2708, MM2716, and 2732 (or 2532) respectively.
- Memory expansion to 64K bytes using any combination of RAM/ROM memory boards.
- On-board RAM memory addressing in the range of $3E00_{16}$ to $3FFF_{16}$.
- On-board EPROM/ROM memory addressing in the range of 0000_{16} to $1FFF_{16}$.

Input/Output

- Parallel I/O

  The BLC-80/05 contains 22 programmable parallel I/O lines implemented using the I/O ports of the 8155 RAM/IO/TIMER. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports (as indicated in Appendix B). Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a 50 contact edge connector.

- Serial I/O

  The BLC-80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the 8085 CPU. These functions are controlled exclusively by software through execution of the 8085 RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Serial I/O signals are TTL compatible, and sockets are provided on the board for optional connection of RS232C line drivers and receivers.

Interval Timer

The BLC-80/05 provides a fully programmable binary 14-bit interval timer utilizing the 8155 RAM/IO/TIMER. Four functions are availble:

- Programmable one-shot
- Square wave rate generator
- Interrupt on termination of a specified count
- Rate generator

Interrupt System

The BLC-80/05 utilizes the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed via a jumper matrix to the four interrupt inputs of the 8085A (TRAP, RST 7.5, RST 6.5, RST 5.5 in order of descending priority). Each input generates a unique memory address (see Table 1). A single 8085 jump instruction at each of these addresses then provides linkage to each interrupt service routing located anywhere in memory. All interrupt inputs with the exception of TRAP can be masked via software. Twelve interrupt sources are provided:

8 — system bus
2 — 8155 I/O ports
1 — 8155 timer
1 — external (available at connector J1)

Table 1

Interrupt Input	Memory Address	Priority	Type
TRAP	24_{16}	Highest	Non-maskable
RST 7.5	$3C_{16}$		Maskable
RST 6.5	34_{16}		Maskable
RST 5.5	$2C_{16}$	Lowest	Maskable

System Bus Arbitration

The Series/80 system allows multiprocessing. Each bus master attached to the bus provides multi-master bus arbitration logic to prevent contention errors. When used in combination, arbitration logic elements on each of the bus masters are interconnected to form a dynamic master/slave relationship.

This logic can be connected in a straight-line priority scheme where bus control is granted in daisy-chaining fashion from the highest to the lowest priority. Any bus master taking control of the bus thereby denies it to the lower priority bus masters in the chain. Using the straight-line priority scheme, there may be up to six masters on a single bus. By using off-board logic, as many as sixteen bus masters are possible. Control of the bus can be gained on a need basis, or permanently via a hardware or software override feature.

BLC-8908 System Monitor Firmware

The BLC-8908 system monitor is availble in a pre-programmed MM2716 PROM. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Routines are included to load or save programs using paper tape. It permits the insertion of break points to facilitate debugging. Programs may be executed starting at any location, or single-stepped. A baud rate search capability is built in which automatically determines the baud rate of the terminal being used at initialization.

The commands supported by the BLC-8908 System Monitor are:

- D — Display memory in hex
- G — Execute program (optionally specify new starting address or breakpoint locations)
- I — Insert into memory
- M — Move memory
- N — Single step
- R — Read hex tape
- S — Examine memory and modify if desired
- W — Punch hex tape
- X — Examine CPU registers and modify if desired

BLC-8959 Serial Cable/Connector Kit

A five-foot RS232C cable and a user-installed connector are available to implement a serial interface.

Specifications

Microprocessor

CPU —	8085A (for instruction set, see Appendix A)
Data Word —	8 bits
Instruction — Word	8, 16, and 24 bits
Cycle Time —	2.03 microseconds (minimum instruction time)
System Clock —	1.996 MHz ± 0.1%
Registers —	6 general purpose, 8-bit accumulator, 8-bit program counter, 16-bit stack pointer
Number of Instructions —	113
Address Capability —	64K bytes

Memory

RAM —	512 bytes on-board
ROM —	Sockets for 8K bytes on-board (ROM/EPROM)
Expansion —	Memory boards in any mix of RAM and ROM up to a 64K byte maximum
Access Time —	500 nanoseconds

Input/Output

Interrupts —	4 level hardware vectored interrupts, 3 maskable
Parallel —	22 programmable I/O lines Latched, unlatched, strobed modes 3- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible Compatible I/O Driver Modules (I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

TYPE	OUTPUT	CURRENT (MA)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Compatible I/O Terminator Modules —	BLC-901 220/330 ohm divider BLC-902 1k ohm pull-up
Serial —	SID and SOD functions of the 8085 CPU are used for serial I/O. They are software controlled through RIM and SIM instructions. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements. Ouputs are TTL compatible. Sockets provided for RS232C line drivers and receivers. Compatible drivers and receivers: Driver — National DS1488 or TI SN75188 Receiver — National DS1490 or TI SN75189
System Bus —	Multiple bus master capability for up to 6 masters, expandable to 16 masters with an external priority network. All address, data, and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

Interval Timer

Clocks —	1 programmable
Size —	14 bits
Interval —	8.14 microseconds to 133.33 milliseconds
Frequency Variation —	7.50 Hz to 61.44 KHz

Connectors

System Bus —	86 contact double-sided card edge connector on 0.156 inch centers
Parallel I/O —	50 contact double-sided edge connector on 0.1 inch centers. Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	7 pin right-angle connector on 0.156 inch centers (male and female required) Recommended connector:

MOLEX	09-65-1071	(male)	09-50-7071	(female)
	08-50-0106	(pin)	15-04-0219	(key)
AMP	87194-6	(male)	3-87025-4	(female)
	87023-1	(pin)	87116-2	(key)

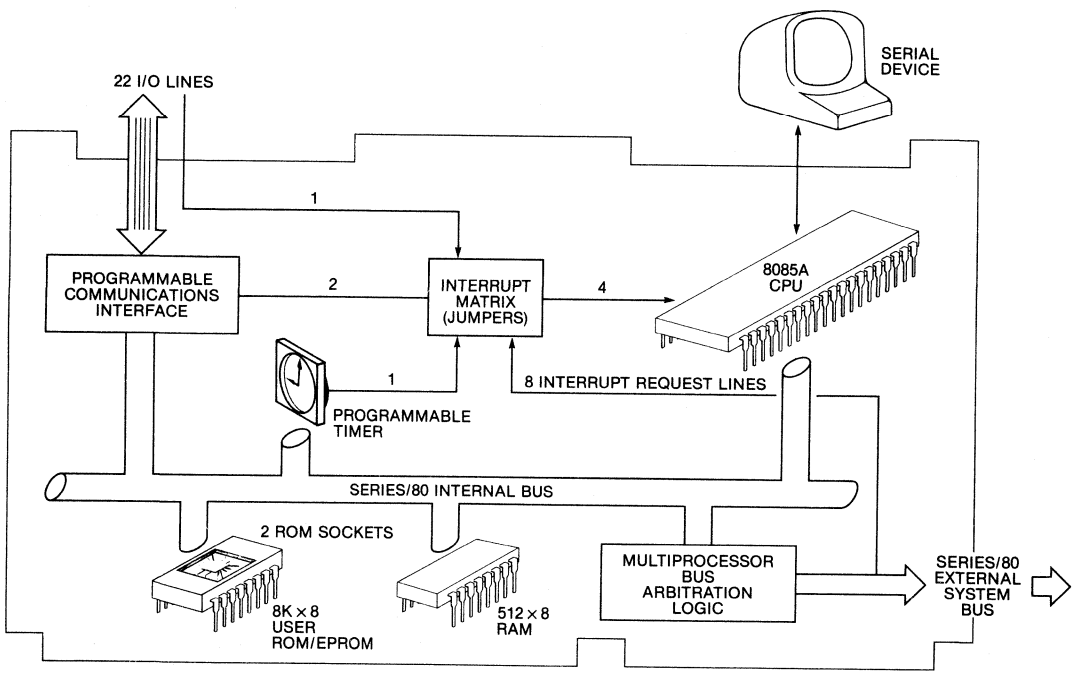
Power	+5V ± 5%, 2.65 A +12V ± 5%, 7 mA −12V ± 5%, 23 mA (includes 2 MM2716 EPROMs and BLC-901 terminators installed for 22 input ports with inputs low; ± 12V required only for RS232C capability)		
Environmental Temperature —	0° to 55 °C Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12.0 oz.	(339.8 gm)

Order Information

BLC-80/05 Series/80 Micro-computer	Includes CPU, 512 bytes of static RAM, sockets for 8K bytes of EPROM, 22 parallel I/O lines, and a serial I/O port

Documentation

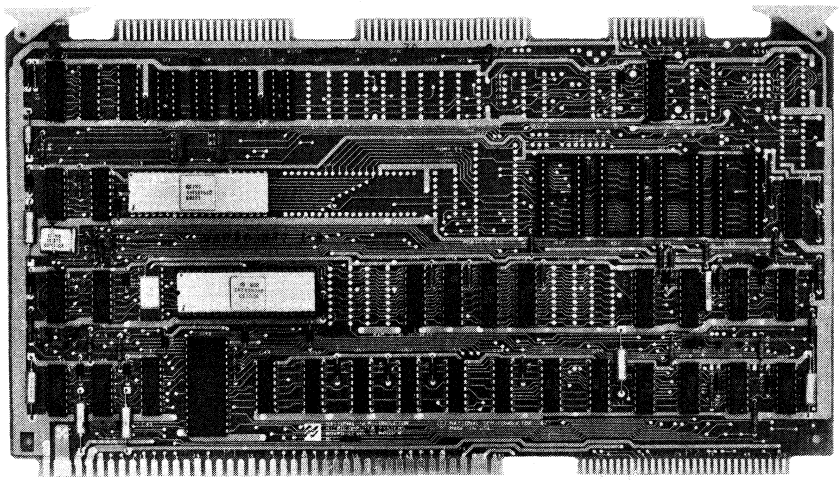
420305817-001	BLC-80/05 Board Level Computer Hardware Reference Manual



BLC-80/05 DIAGRAM

National Semiconductor

BLC-80/07
Series/80 Board Level Computer



- **Low Cost with BLC/SBC-80/10 Computing Power**
- **24 Programmable Parallel I/O Lines — Fits Most Control Applications**
- **488 ns Memory Access Time for Fast Operation**
- **Compatible with BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 4 Interrupt Lines
  - 512 Bytes of RAM
  - 4K Bytes of PROM
  - 64K Byte Addressing

Product Overview

The BLC-80/07 is a self-contained single board computer with the computing power of a BLC-80/10 computer. Based on the 8080A microprocessor, the BLC-80/07 is totally compatible with the wide range of BLC/SBC Series/80 hardware and software products.

The BLC-80/07 is a complete computer including a CPU, 24 parallel I/O lines, 512 bytes of static random access memory (RAM), sockets to accept 4K bytes of read only memory (ROM) and a system clock. The basic BLC-80/07 may be expanded in many dimensions through the addition of other products in the BLC/SBC Series/80 family, such as four slot chassis, power supply, RAM and ROM memory in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

The primary advantage of the BLC-80/07 is that it is a very low cost single board computer capable of solving a wide variety of applications problems, yet is expandable with standard Series/80 products at a reasonably low incremental cost.

Functional Description

Central Processor

- CPU: 8080A Microprocessor
- Maximum addressing range — 64K bytes
- Data word — 8 bits
- Instruction word — 8, 16 or 24 bits
- Addressing modes — direct, register, register indirect and immediate

- Instruction types — a total of 111
  - — 18 Data Transfer
  - — 29 Arithmetic
  - — 19 Logical
  - — 29 Branch
  - — 16 Control
- Registers
  - — 7 General Registers — 1 accumulator (A) plus six 8-bit work registers which may be utilized individually (B, C, D, E, H and L) or in pairs (B and C, D and E, H and L), effectively forming 16-bit registers.
  - — 1 16-bit Program Counter
  - — 1 16-bit Stack Pointer
  - — Sub-Routine Mechanism utilizes the stack pointer with push and pop instruction to implement "Call" and "Return" instruction types
- Sub-Routine Mechanism
  - — Hardware stack pointer with push and pop instructions
  - — Call and return instructions

Memory

512 bytes of static read write RAM is available on-board. The RAM is implemented using MM2111 memory modules. On-board memory addressing is predefined in the range 3E00 through 3FFF.

Sockets are installed on the computer to allow user implementation of read only memory for the specific application. The ROM section of the computer accepts 4K bytes of ROM using low cost MM2708 EPROM's. On-board ROM memory addressing is predefined in the range 0 through $0FFF_{16}$.

Memory expansion is possible using any mix of RAM and ROM memory expansion boards up to a maximum of 64K bytes. All expansion memory boards may be jumper selected for addressing in the range 0 through $FFFF_{16}$. This permits simple system integration.

Input/Output

The 24 input/output lines are controlled by an INS8255 Programmable Peripheral Interface circuit. Using standard Series/80 instructions, the 24 lines may be configured to a variety of unidirectional/bidirectional modes. The operating modes are defined in Appendix B.

- Interrupts
  - — 1 level with 4 individual lines
- Parallel
  - — 24 programmable I/O lines
  - — Latched, unlatched, strobed modes
  - — 8-bit parallel configuration
  - — Optional line drivers and terminators
  - — TTL compatible
- Compatible I/O Driver Modules
  - — A variety of driver circuit types are available for use in the input/output section: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps.

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (ma)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

- Compatible I/O Terminator Modules
  - — BLC-901 220/330 ohm divider
  - — BLC-902 1K ohm pull-up

System Bus

All address, data and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

The input/output section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14 pin DIP packages. All drivers are TTL compatible. Two of the 3 parallel I/O ports are available for user implementation of appropriate driver circuits. Port number 1 has permanently installed 8226 type drivers.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

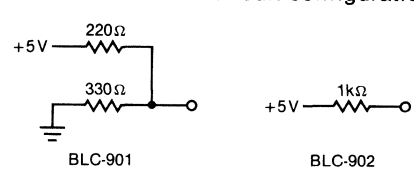


Figure 1. BLC-901 and BLC-902 Terminators

Interrupt

The CPU has a single level interrupt for recognition of events. Interrupts may originate from four sources OR-tied to the single level. When an interrupt is received, an in-process instruction is completed and then the program is suspended. The CPU passes control to a user defined interrupt service routine which saves system conditions while the interrupt is processed. Interrupt processing starts from location 0038_{16}.

Specifications

Microprocessor

CPU —	8080A (for Instruction Set, see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16 and 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	512 bytes on-board
ROM —	Sockets for 4K bytes on-board
Expansion —	Memory boards in any mix of RAM and ROM up to a 64K bytes maximum
Access Time —	500 nanoseconds (maximum)

Connectors

System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary —	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559 TI H311130
Parallel I/O —	50 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3

Power	+5V, 2.2A −5V, 0.02A +12V, 0.15A −12V, 0.15A
Environmental	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing

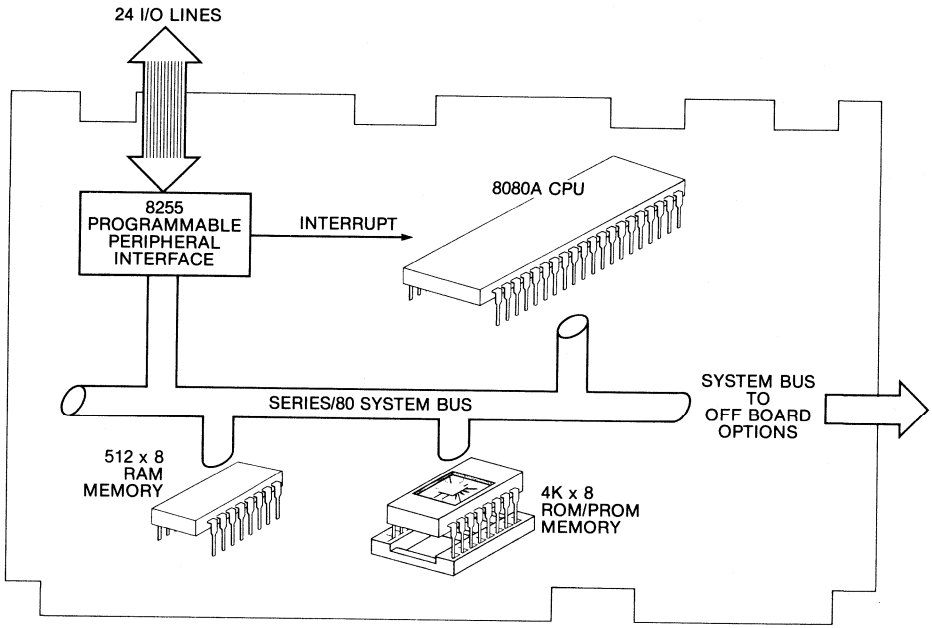
Physical		
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/07	Series/80 Microcomputer Includes CPU, 512 bytes of static RAM, sockets for 4K bytes of ROM and 24 parallel I/O lines.

Documentation

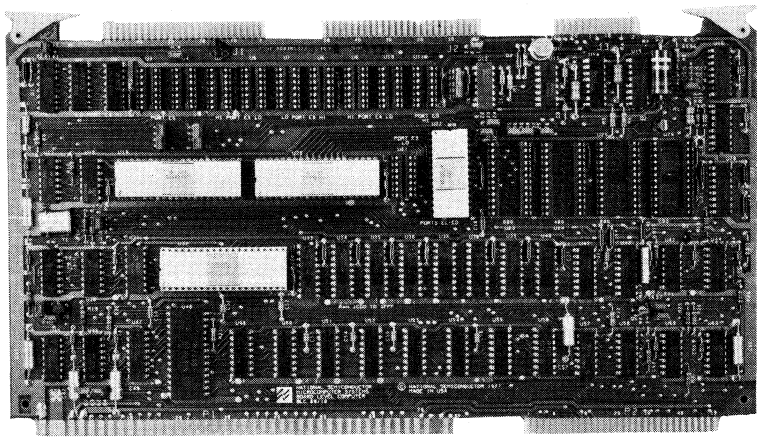
420305373-001	BLC-80/07, 10 Board Level Computer Hardware Reference Manual



BLC-80/07 Diagram

National Semiconductor

BLC-80/10
Series/80 Board Level Computer



- **Low Cost Computing Power**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K static RAM
  - 4K ROM/PROM
- **48 Programmable Parallel I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **Plug-replacement for Intel SBC-80/10**

Product Overview

The BLC-80/10 is a self contained Board Level Computer based on the INS8080A LSI microprocessor. The BLC-80/10 is functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/10 is a complete computer including a CPU, a serial communications interface, 48 parallel I/O lines, 1K bytes of static Random Access Memory (RAM), sockets to accept 4K bytes of Read Only Memory (ROM/PROM) and a system clock. The BLC-80/10 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/10 contains 1K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range $3C00_{16}$ to $3FFF_{16}$.

Sockets are installed to allow user implementation of read only memory for the specific application. Up to 4K bytes of ROM can be installed in 1K increments. MM2308 ROM's or low cost MM2708 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

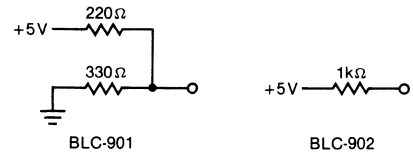


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2 KHz	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

The BLC-80/10 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4

interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080A (for Instruction Set see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16, 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	1K bytes on-board
ROM —	Sockets for 4K bytes
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes maximum
Access Time —	500 nanoseconds (maximum)

Input/Output

Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card cage edge connector on 0.156-inch centers
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round

Power

+5V, 2.9A
−5V, 0.002A
+12V, 0.14A
−12V, 0.18A
(excluding power required for I/O drivers and user supplied PROM's)

Environmental

Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical

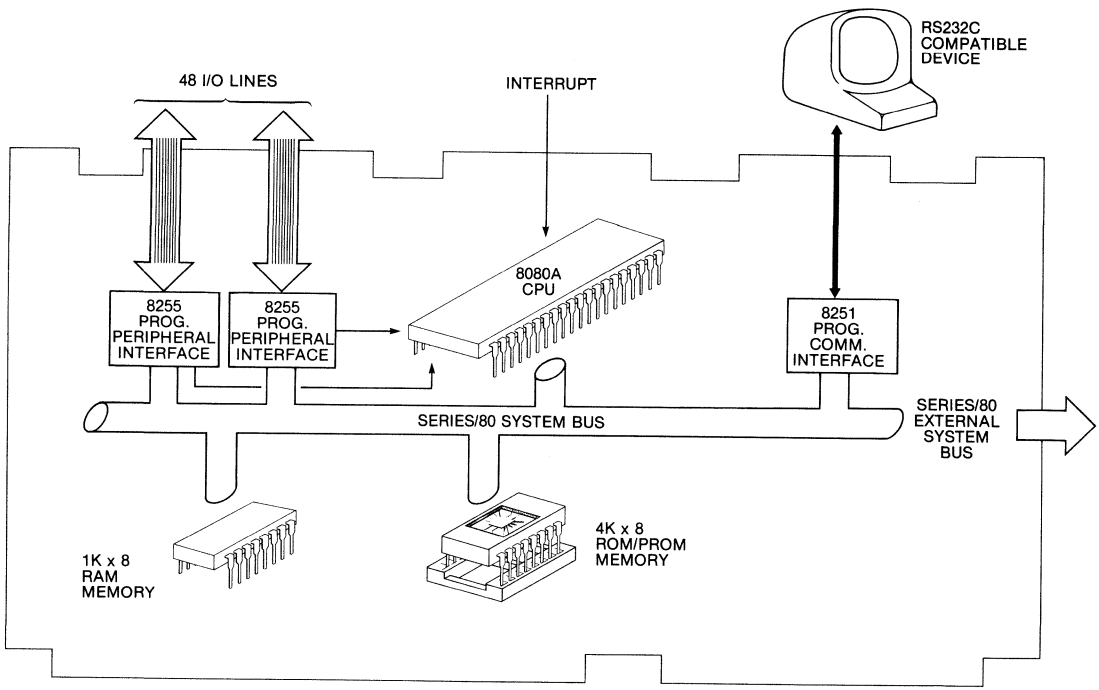
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/10	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K bytes of ROM, 48 parallel I/O lines and a serial communications interface.

Documentation

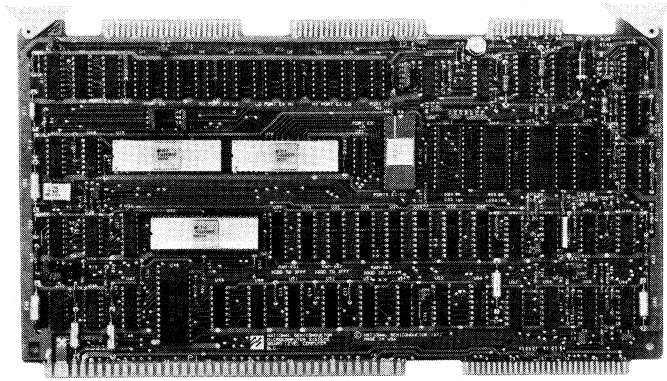
420305373-001	BLC-80/10 Board Level Computer Hardware Reference Manual



BLC-80/10 Diagram

National Semiconductor

BLC-80/11, BLC-80/12, BLC-80/14 Series/80 Board Level Computer



- **Low Cost Computing Power with Expanded On-Board Memory**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K, 2K, 4K static RAM
  - UP TO 8K ROM/PROM
- **48 Programmable I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **RS232C Interface Selectable for Data Set or Data Terminal**
- **Plug-replacement for Intel SBC-80/10A**

Product Overview

The BLC-80/11, 80/12, and 80/14 are self contained Board Level Computers based on the INS8080A LSI microprocessor. These computers are functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/11, 80/12, and 80/14 are complete computers including a CPU, a serial communications interface, 48 parallel I/O lines, up to 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. These computers may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

The primary advantage of the BLC-80/11, 80/12, and 80/14 over the BLC-80/10 is their increased RAM and ROM capacity.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/11, 80/12, and 80/14. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11, 80/12 and 80/14 contain 1K, 2K, or 4K bytes, respectively, of on-board static RAM implemented with MM2114 memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending upon the amount of RAM installed.

Four sockets are installed to allow user implementation of read only memory for the specific application. Jumpers are provided to allow the use of MM2308/MM2316E ROM's or MM2708/MM2716 EPROM's, giving a maximum of 8K bytes of read only memory in 1K or 2K increments. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending upon the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

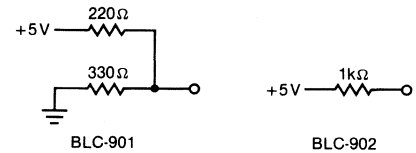


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2 KHz	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

The BLC-80/11, 80/12, and 80/14 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080A (for Instruction Set see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16, 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	BLC-80/11	1K bytes
	BLC-80/12	2K bytes
	BLC-80/14	4K bytes
ROM —	Sockets for up to 8K bytes	
RAM Memory Addressing —	BLC-80/11	$3C00_{16}$ to $3FFF_{16}$
	BLC-80/12	3800_{16} to $3FFF_{16}$
	BLC-80/14	3000_{16} to $3FFF_{16}$
ROM Memory Addressing —	0000 to $0FFF_{16}$ or $1FFF_{16}$	
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes maximum	
Access Time —	500 nanoseconds (maximum)	

Input/Output

Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card cage edge connector on 0.156-inch centers
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round

Power

+5V, 2.9A
−5V, 0.002A
+12V, 0.14A
−12V, 0.18A
(excluding power required for I/O drivers and user supplied PROM's)

Environmental

Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical

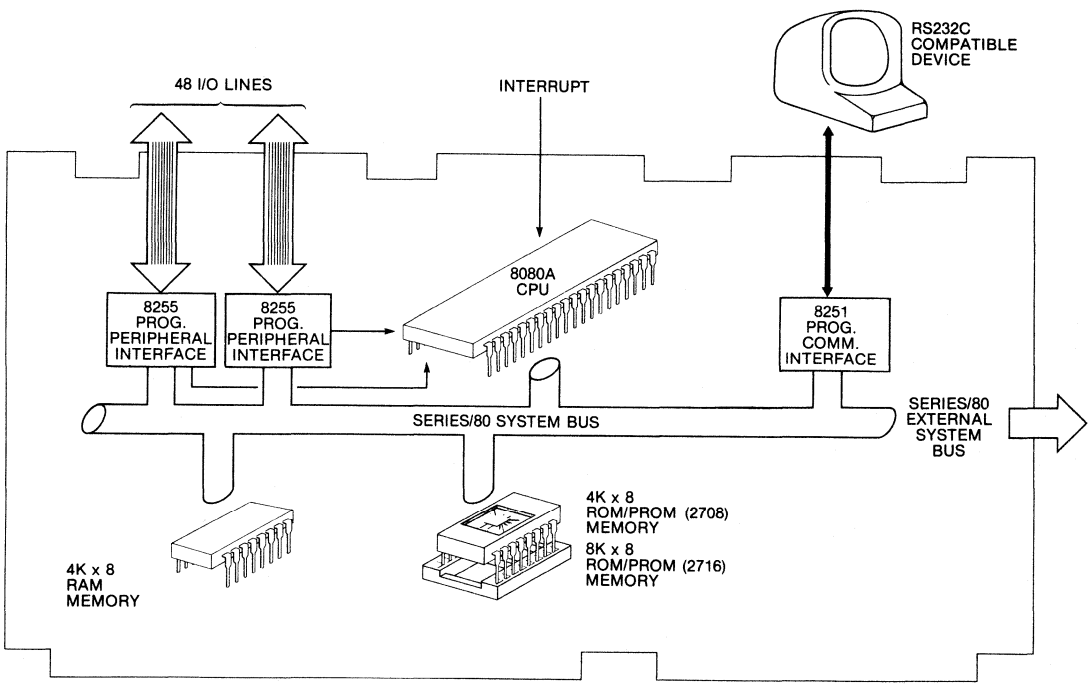
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/11	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines and a serial communications interface.
BLC-80/12	Series/80 Microcomputer Includes CPU, 2K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and a serial communications interface.
BLC-80/14	Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and serial communications interface.

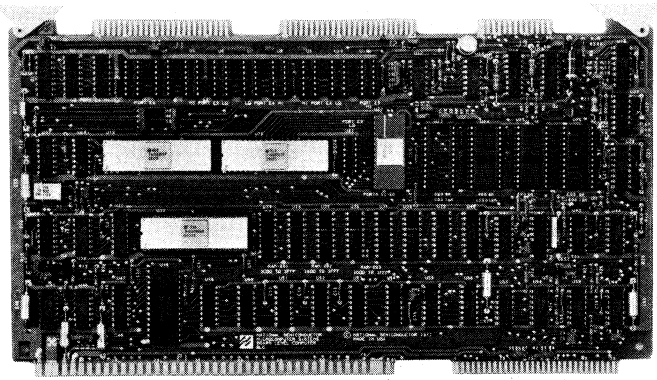
Documentation

420305532-001	BLC-80/11, 80/12, 80/14 Board Level Computer Hardware Reference Manual



BLC-80/14 Diagram

BLC-80/11T, BLC-80/12T, BLC-80/14T Series/80 Board Level Computer (Extended Temperature Range)



- **Extended Operating Temperature Range of −40°C to +85°C (−40°F to +185°F)**
- **Low Cost Computing Power with Expanded On-Board Memory**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
- **48 Programmable I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **RS232C Interface Selectable for Data Set or Data Terminal**
- **Plug-replacement for Intel SBC-80/10A**

Product Overview

The extended temperature range series of CPU boards, BLC-80/11T, 80/12T, and 80/14T are intended for use in environments that require operating ranges of −40°C to +85°C. The components used on these boards are specially selected for their extended operating range. The boards are dynamically tested for 48 hours, repeatedly cycling between the temperature extremes, as part of the National Quality/Reliability Program. The extended temperature versions are form, fit, and functionally compatible in all respects with our standard BLC-80/11, 80/12 and 80/14 CPU boards.

The BLC-80/11T, 80/12T and 80/14T are complete computers including a CPU, a serial communications interface, 48 parallel I/O lines, up to 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. These computers may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

Central Processor

The INS8080ADI n-channel LSI microprocessor (extended temperature version of INS8080A) is the central processor for the BLC-80/11T, 80/12T, and 80/14T. The INS8080ADI contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11T, 80/12T, and 80/14T contain 1K, 2K, or 4K bytes, respectively, of on-board static RAM implemented with AM9114DM memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending upon the amount of RAM installed.

Four sockets are installed to allow user implementation of read only memory for the specific application. Jumpers are provided to allow the use of AM9208BDM/AM9216BDM ROMs or ID2708/ ID2716 EPROMs, giving a total of up to 8K bytes of read only memory in 1K or 2K increments. Addressing of the ROM/PROMs is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending upon the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two AM9555DM Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional latched/ unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed AM8226 type drivers. Figure 1 illustrates the I/O address assigned to the AM9555 PPIs.

	9555 No. 1				9555 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E9	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules, as well as a number of TTL devices, are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table I lists the compatible driver modules.

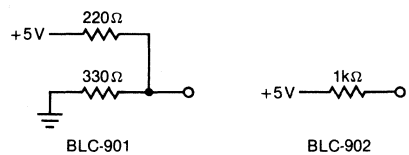


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One AM9551DM Universal Synchronous/ Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table II lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2 KHz	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

The BLC-80/11T, and 80/14T can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the AM9555DM PPI devices signifying input buffer full or output buffer empty
- 2 from the AM9551DM USART device signifying input data ready or output character needed

The interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080ADI (for Instruction Set see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16, 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	BLC-80/11T	1K bytes
	BLC-80/12T	2K bytes
	BLC-80/14T	4K bytes
ROM —	Sockets for up to 8K bytes	
RAM Memory Addressing —	BLC-80/11T	$3C00_{16}$ to $3FFF_{16}$
	BLC-80/12T	3800_{16} to $3FFF_{16}$
	BLC-80/14T	3000_{16} to $3FFF_{16}$
ROM Memory Addressing —	000 to $0FFF_{16}$ or $1FFF_{16}$	
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes	
Access Time —	500 nanoseconds (maximum)	

Input/Output

Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card card edge connector on 0.156-inch centers Recommended mating connector: CDC VPB01E43D00A1 Viking 2VH43/1AV5
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round
Card Guides —	EECO KG 375
Power —	+5V, 2.9A −5V, 0.002A +12V, 0.14A −12V, 0.18A (excluding power required for I/O drivers and user supplied PROMs)

Environmental — Temperature −40°C to +85°C
Humidity 0 to 90% non-condensing

Physical —

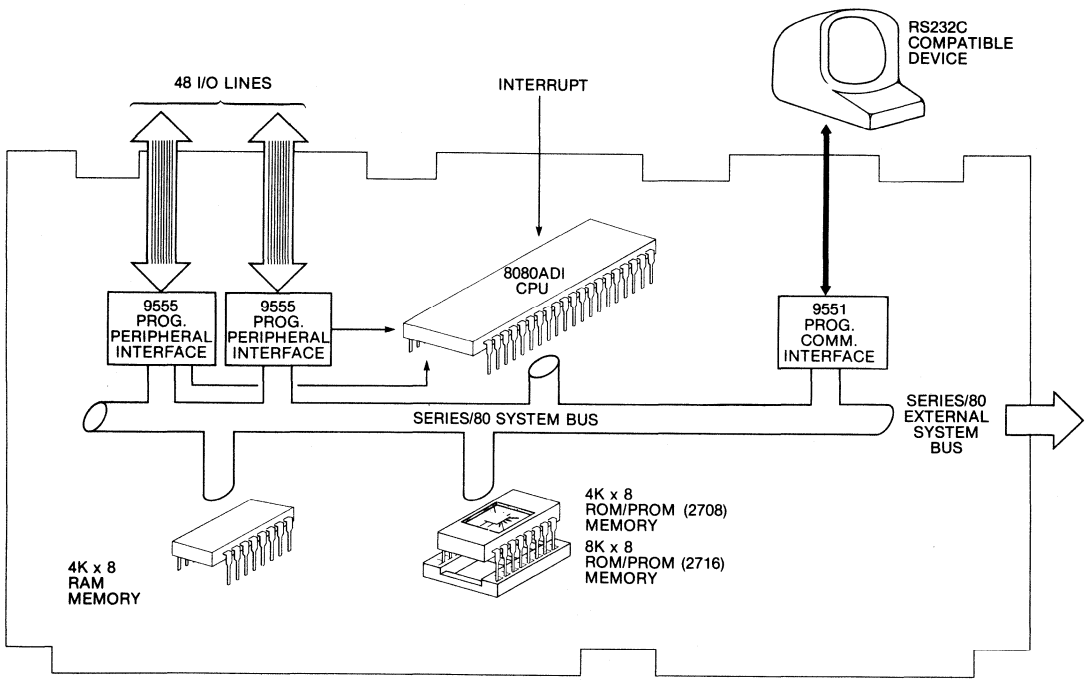
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 gm)

Order Information

BLC-80/11T	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines and a serial communications interface.
BLC-80/12T	Series/80 Microcomputer Includes CPU, 2K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and a serial communications interface.
BLC-80/14T	Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and a serial communications interface.

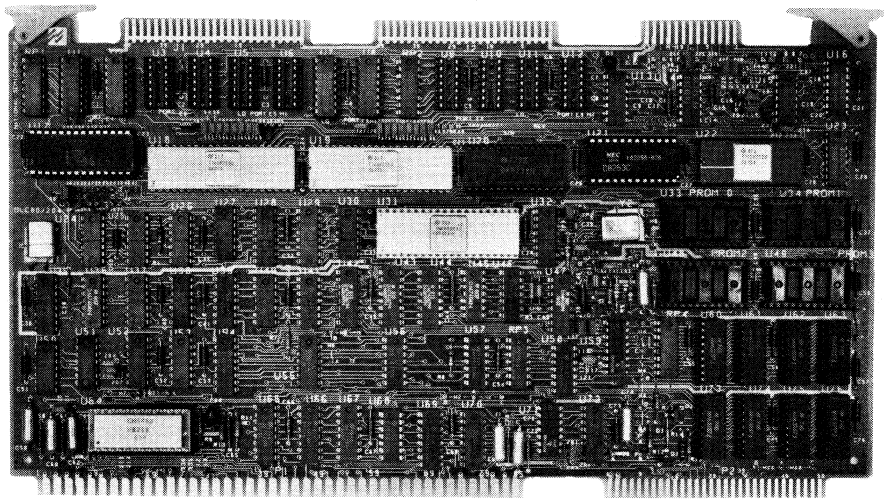
Documentation

420305532-001	BLC-80/11, 80/12, 80/14, 80/11T, 80/12T, 80/14T Board Level Computer Hardware Reference Manual



BLC-80/14T DIAGRAM

BLC-80/204
Series/80 Board Level Computer



- **Complete System Capability, including:**
  - 8 vectored interrupts
  - Multiple processor capability — up to six bus masters
  - Interval timer with three programmable counters
  - ROM/RAM "shadowing" capability under software control
  - Larger memory — 4K bytes RAM and sockets for up to 8K bytes of EPROM/ROM
  - Programmable RS232C communications interface with program selectable baud rates
- **Low Power MM5257 Static RAM with Battery Backup Circuitry**
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
- **Plug-for-Plug Compatible with the Intel SBC-80/20 and SBC-80/204**

Product Overview

The BLC-80/204 is a self-contained board level computer with 4K bytes RAM. System features on the BLC-80/204 allow building more complex and powerful systems including multi-processor configurations. Based upon the 8080A-2 microprocessor, the BLC-80/204 incorporates special Series/80 bus arbitration logic to sort out contention disputes among several processors sharing the same system bus.

Minicomputer systems concepts widely accepted among computer systems builders, such as vectored interrupts, have been incorporated into the BLC-80/204. Vectored interrupts is a hardware technique that automatically handles all the necessary details of identifying the interrupts, storing the status of the CPU, and initiating the interrupt service routine. This technique is superior to the software polling scheme of non-vectored CPU's since it eliminates unnecessary cycling through a software polling routine to determine which interrupt to service.

Microcomputer industry concepts, such as a single chip Universal Synchronous/Asynchronous Receiver/Transmitter (USART), are included. The USART features include a vast number of transmission rates, from 110 to 38,400 baud, all under program control.

The BLC-80/204 is a complete computer including:

- CPU
- Serial I/O
- Parallel I/O
- Interval timers
- Vectored interrupts
- RAM and ROM memory

The basic BLC-80/204 microcomputer can be expanded by the addition of a four slot chassis, power supply, ROM and RAM memory, various I/O controllers, analog and digital I/O and other system modules — even more BLC-80/204's. Thus, the basic advantage of the BLC-80/204 is that it provides low cost single board computer capability, yet is expandable to a substantially more powerful multiprocessor configuration.

Functional Description

Central Processor

- CPU: 8080A-2 Microprocessor
- Maximum addressing range — 64K bytes
- Data word — 8 bits
- Instruction word — 8, 16, 24 bits
- Addressing modes — direct, register, register indirect and immediate
- Instruction types — total of 111 instructions
  - — 18 data transfer
  - — 29 arithmetic
  - — 19 logical
  - — 29 branch
  - — 16 central
- Registers
  - — 7 general registers — 1 accumulator (A) plus six 8-bit work registers which may be utilized individually (B, C, D, E, H, L) or in pairs (B and C, D and E, H and L), effectively forming three 16-bit registers.
  - — 1 16-bit program counter.
  - — 1 16-bit stack pointer.
- Subroutine mechanism
  - — Hardware stack pointer with push and pop instruction
  - — Call and return instructions

Memory

- 4K bytes of static read/write memory using MM5257 RAM with auxiliary battery backup power bus (560 ma, 1.5 V)
- Sockets on-board for up to 8K bytes of ROM in 1K or 2K increments using MM2708 or MM2716 EPROM
- Memory expansion to 64K bytes using any combination of RAM/ROM memory boards
- A memory shadow technique is incorporated allowing on-board ROM memory addresses to be identical to off-board ROM/RAM memory addresses. By switching back and forth via software, a ROM bootstrap routine can "disappear" from memory to be replaced with RAM once the system start-up procedure is past the bootstrap stage.
- On-board RAM memory addressing in the range 2000_{16} through $FFFF_{16}$ selectable on 4K byte boundaries. Off-board RAM memory addressing from 0000 to $FFFF_{16}$.
- ROM/PROM memory addressing in the range 0000 through $1FFF_{16}$.
- An automatic synchronizing signal is generated by the processor during non-memory access time periods to allow the off-board dynamic RAM expansion memory to go through a refresh cycle without reducing system throughput. This unique refresh synchronizing technique effectively allows the dynamic expansion memory to exhibit static memory characteristics.

Input/Output

- Parallel I/O
  - — Two INS8255 programmable peripheral interface circuits provide a total of 48 I/O lines which can be configured by software into any combination of unidirectional/bidirectional I/O ports. Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a pair of 50 contact edge connectors for mating with cables. The operating modes are defined in Appendix B.
- Serial I/O
  - — One INS8251 Universal Synchronous/Asynchronous Receiver/Transmitter provides the serial I/O port with programmable communications rates, data formats, control characters and parity. Logic is provided for detection of framing, overrun and parity errors, as well as double buffering. The serial I/O port provides RS232C signals interfaced via a 26 contact edge connector.

Interval Timer (Clocks)

One 8253 programmable interval timer provides three programmable 16-bit counters. One is used as a baud rate generator for the serial I/O port and

the other two are used as general purpose BCD or binary 16-bit counters. The other two can be cascaded into one 32-bit counter. Each clock has up to seven software selectable functions:

- Interrupt on termination of a specified count
- Programmable one-shot
- Rate generator based upon a multiple of the input clock period
- Square wave rate generator
- Software triggered strobe
- Hardware triggered strobe
- Event counter (using external signal to drive clock input)

Input Frequencies —	Reference 1.0752 MHz ± 0.1% Event rate 1.1 MHz maximum
Output Frequencies/ Timing Intervals —	Variable time intervals from 1.86 microseconds to 1.109 hours. Frequency variation from 25 KHz to 537.61 KHz.

Interrupt System

A programmable interrupt module handles interrupt vectoring of eight interrupt levels. Four priority processing modes may be reconfigured under program control during system operation. Interrupts in any combination may be masked under program control.

The programmable interrupt module accepts interrupts from parallel and serial I/O, programmable timers, or the system bus. Each interrupt is serviced based on its priority, which is determined by attaching the device interrupt line to one of eight system bus interrupt lines.

Each of the eight BLC-80/204 levels is connected to a specific line on the system bus. Each level may be connected to as many as 16 interrupts, but the system will not detect more than one interrupt at a time on the same level. A software polling routine may be used to distinguish among multiple interrupts on the same level if more than eight are desired. On-board interrupt sources are available as follows:

4 — two from each of two 8255 parallel I/O modules

2 — two from the 8251 serial I/O module

2 — one from each of two available system clocks

Interrupts may come from up to 8 sources on the Series/80 system bus and up to 48 from the I/O ports on the two 8255's.

A block of memory (32 or 64 bytes) must be reserved for interrupt vectors. The address for each level is spaced at intervals of 4 or 8 bytes (program selectable). A single JUMP instruction at each location links the ultimate service routine.

Table 1. Programmable Interrupt Modes

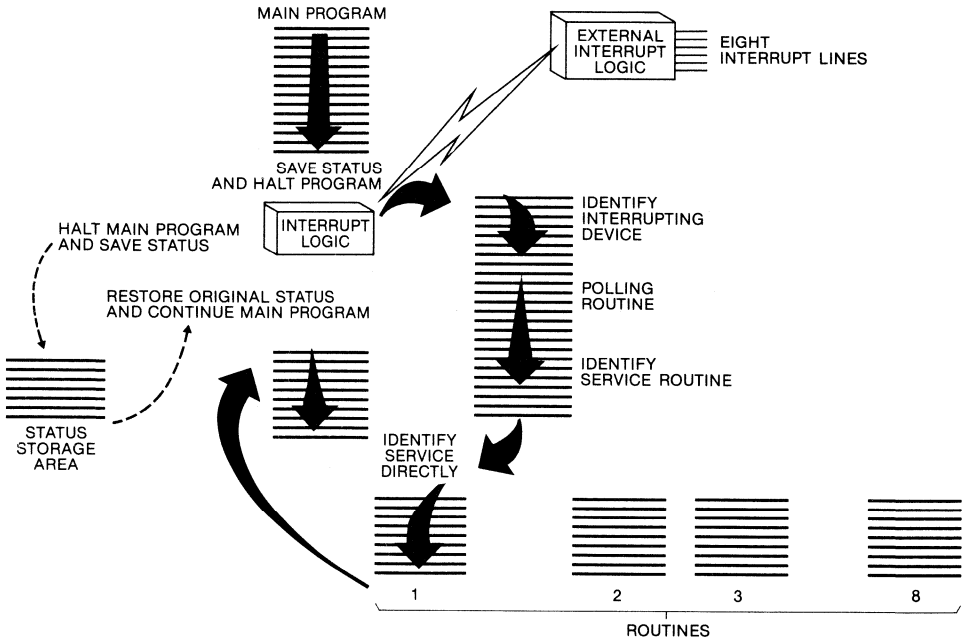
Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 (highest) through 7 (lowest).
Auto-Rotating	Once serviced, a given level becomes the lowest priority level until the next interrupt occurs.
Specific Priority	Software assigns the lowest priority level.
Polled	Software examines an interrupt status by using the interrupt status register.

System Bus Arbitration

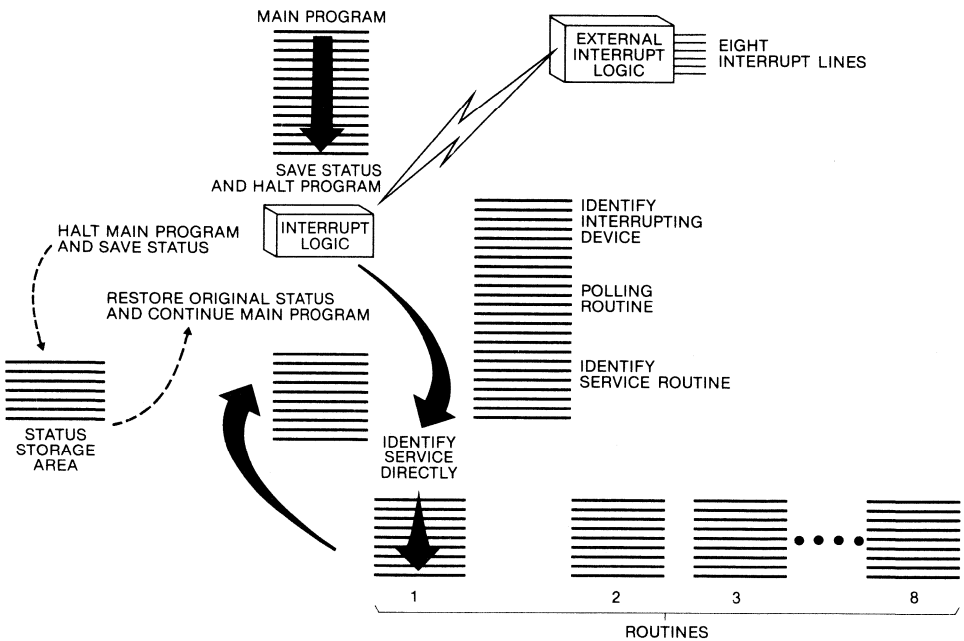
The Series/80 system bus allows multiple devices to transfer data on a common bus.

The Series/80 system bus allows multiprocessing. Each bus master attached to the Series/80 system bus must provide multi-master bus arbitration logic to prevent contention errors. When used in a system configuration, bus arbitration logic elements on each of the bus masters are interconnected to form a dynamic master/slave relationship.

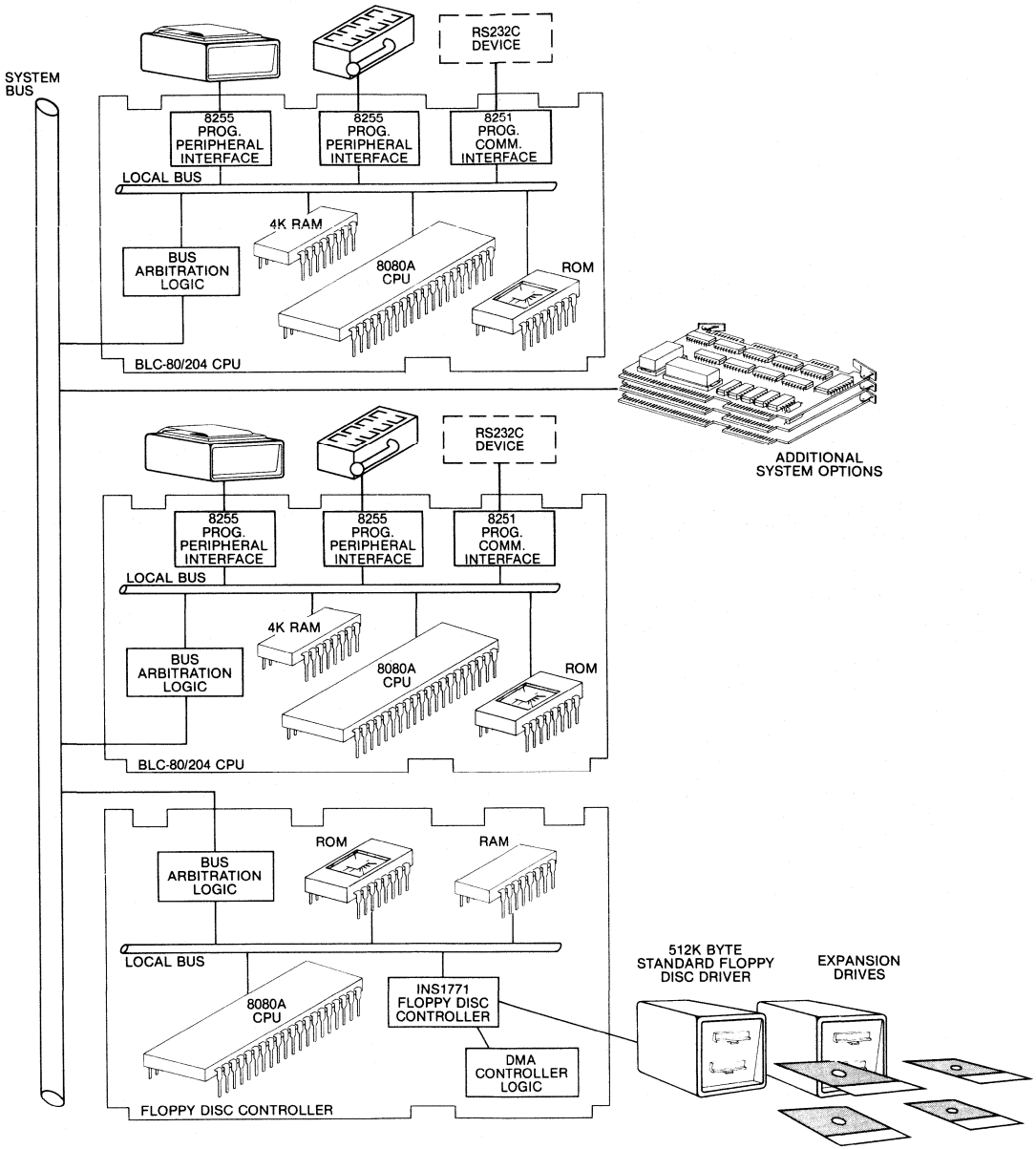
The bus arbitration logic modules can be connected in a straight-line priority scheme where bus control is granted in daisy-chaining fashion from the highest priority to the lowest priority. Any bus master taking control of the bus thereby denies it to bus masters lower in priority in the chain. Using the straight-line priority scheme, there may be up to six bus masters on a single system. By using off-board logic, as many as sixteen bus masters are possible.



Without Vectored Interrupts



Vectored Interrupts



Typical Microprocessor: BLC-80/204 System Diagram

Specifications

Microprocessor

CPU — 8080A-2 (for Instruction Set, see Appendix A)

Data Word — 8 bits

Instruction Word — 8, 16 and 24 bits

Cycle Time — 1.86 microseconds (minimum instruction time)

System Clock — 2.1504 MHz ± 0.1%

Registers — 6 General Purpose, 8-bit
Accumulator, 8-bit
Program Counter, 16-bit
Stack Pointer, 16-bit

Number of Instructions — 111

Address Capacity — 64K bytes

Memory

RAM — 4K bytes on-board

ROM — Sockets for 8K bytes on-board (ROM/PROM/EPROM)

Expansion — Memory boards in any mix of RAM and ROM up to a 64K byte maximum

Access Time — 500 nanoseconds (maximum)

Input/Output

Interrupts — 8 level hardware vectored interrupts
Programmable masking
4 priority modes

Parallel — 48 programmable I/O lines
Latched, unlatched, strobed modes
4- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Compatible I/O Driver Modules
(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (ma)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Compatible I/O Terminator Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial — Programmable
Full data set control
Double buffered
RS232C compatible
Synchronous mode:
- 5-8-bit character
- Internal/external synchronization
- Automatic SYNC insertion
- SYNC search
- 75-9600 baud

Asynchronous mode:
- 5-8-bit character
- 1, 1½ or 2 stop bits
- False start bit detect
- 1760-38400 baud
- Break character generation

System Bus — Multiple bus master capability for up to 6 masters, expandable to 16 masters with additional priority network. All address, data and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

Interval Timer (Clocks)

Clocks — 3 programmable

Size — 16 bits

Interval — 1.86 microseconds to 1.109 hours

Frequency Variation — 25 KHz to 537.61 KHz

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — (Battery back-up) 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Serial I/O — 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power

VDC	Normal	Battery
+5V	4.9A	0.56A
−5V	0.18A	—
+12V	0.35A	—
−12V	0.02A	—

(normal based on 4K ROM installed)

Environmental Temperature 0° to 55°C
Humidity 0 to 90%, non-condensing

Physical

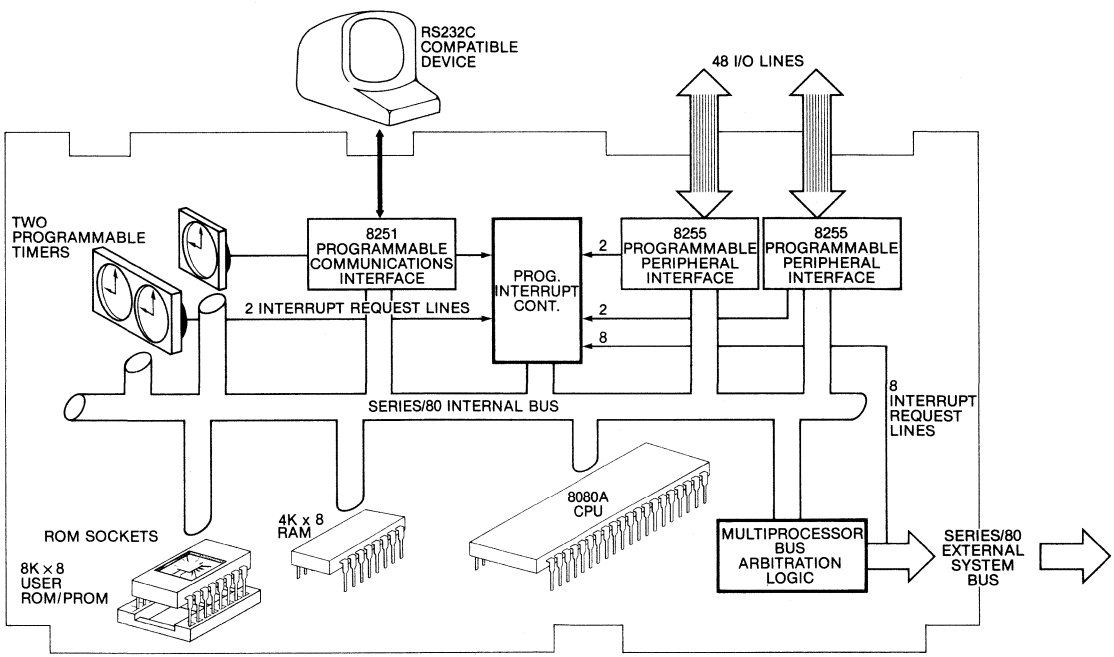
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/204 Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 8K bytes of ROM, 48 parallel I/O lines and an RS232C serial I/O

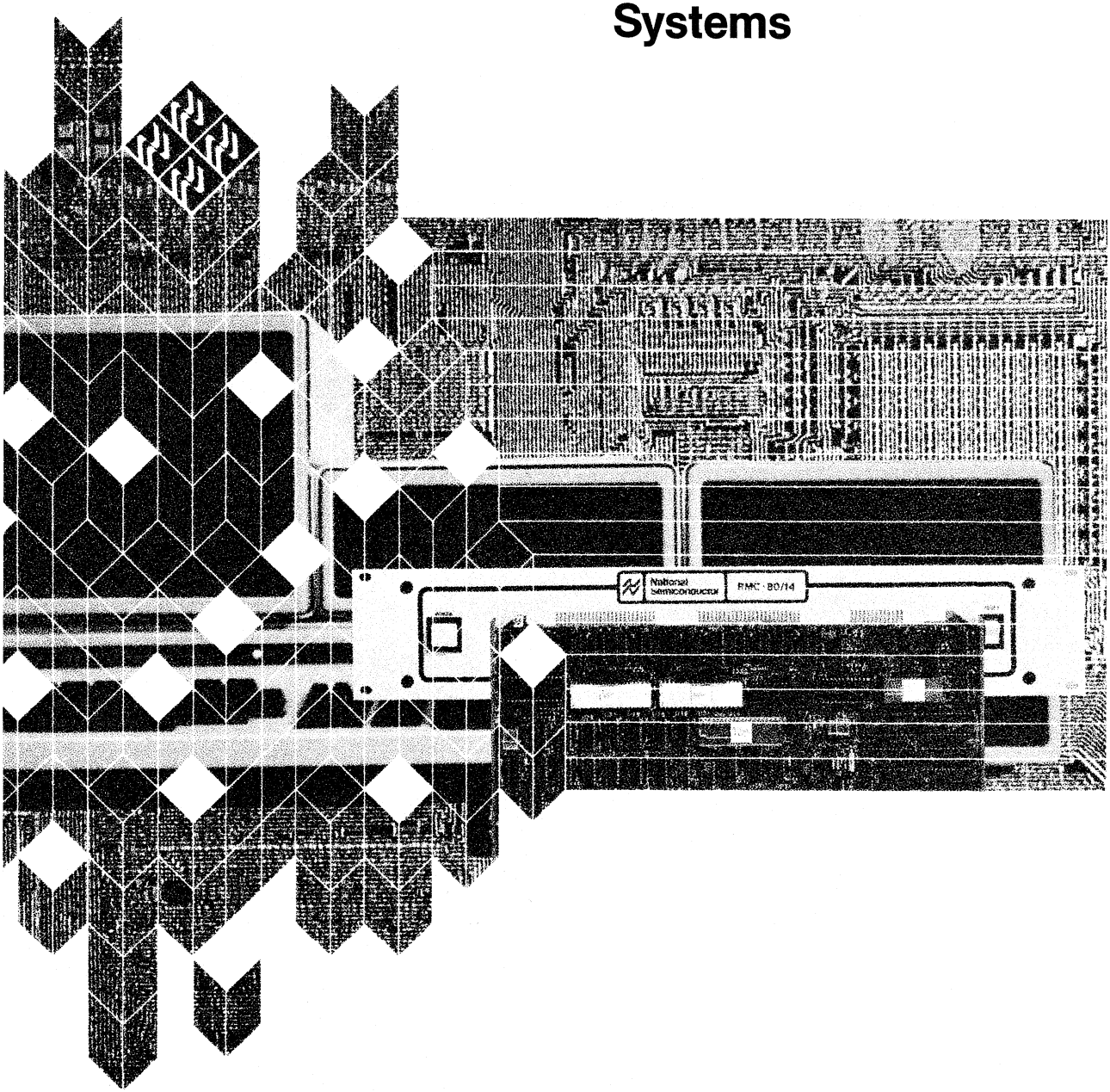
Documentation

420305521-001 BLC-80/204 Board Level Computer Hardware Reference Manual

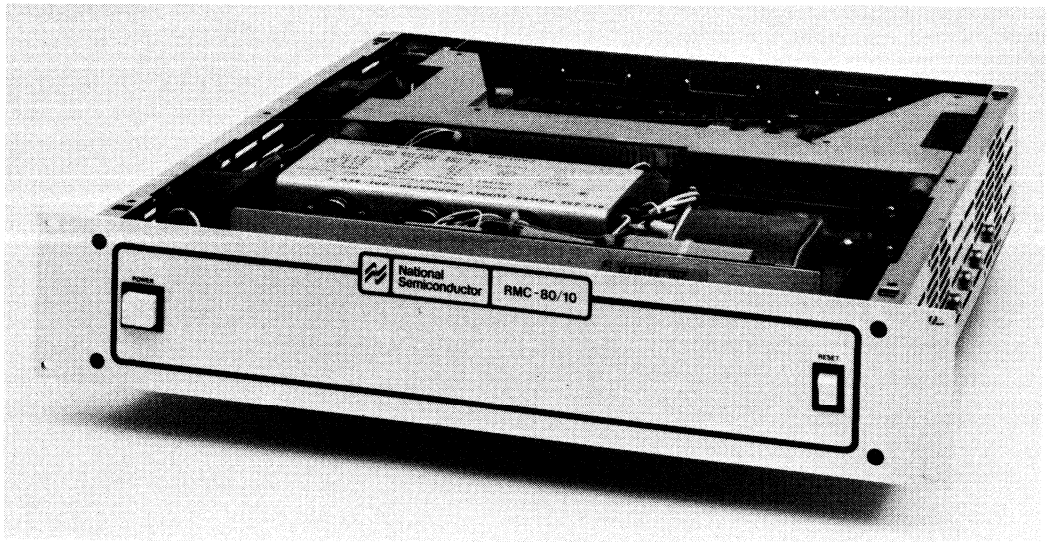


BLC-80/204 Diagram

Section 2
Rack Mountable Microcomputer Systems



RMC-80/10
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/10 Board Level Computer
  - BLC-910 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power and Reset Switches**
- **Rear Panel with D Type Connector Knockouts**
- **Expandable with Standard BLC/SBC Series/80 Products**
- **Replacement for Intel's System 80/10**

Product Overview

The RMC-80/10 is a packaged microcomputer system based on the BLC-80/10 Board Level Computer. The RMC-80/10 occupies only 3½ inches of vertical space in a standard 19-inch RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/10 CPU board plus three additional expansion boards. The 3½-inch chassis contains the CPU board, power supply, fans, and three expansion board slots.

The CPU board in the RMC-80/10 is based on the INS8080A LSI microprocessor. The RMC-80/10 is functionally compatible with the entire family of BLC/SBC hardware and software products.

Installed in the RMC-80/10 is a complete Board Level Computer including a CPU, a serial communications interface, 48 parallel I/O lines, 1K bytes of static Random Access Memory (RAM), sockets to accept 4K bytes of Read Only Memory (ROM/PROM) and a system clock. The RMC-80/10 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/10 CPU

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/10 contains 1K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range $3C00_{16}$ to $3FFF_{16}$.

Sockets are installed to allow user implementation of read only memory for the specific application. Up to 4K bytes of ROM can be installed in 1K increments. MM2308 ROM's or low cost MM2708 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O addresses assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

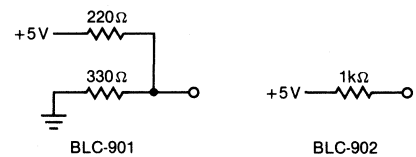


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity.

Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. In the RS232C mode, jumper selection is available to reconfigure the port as either a data set or a data terminal. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Timer Selection	Baud Rate Clock (user selectable software)	Baud Rate (Hz)		
		Synchronous	Asynchronous (program selectable)	
			÷16	÷64
÷7	153.6 KHz	—	9600	2400
÷14	76.8 KHz	—	4800	1200
÷28	38.4 KHz	38400	2400	600
÷56	19.2 KHz	19200	1200	300
÷112	9.6 KHz	9600	600	150
÷224	4.8 KHz	4800	300	75
÷448	2.4 KHz	2400	150	
÷611	1.76 KHz	1760	110	

Interrupt System

The BLC-80/10 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

BLC-910 System Monitor Firmware

Two MM2708 PROM's containing the system monitor are installed in the BLC-80/10. The monitor can be used for loading, debugging, and executing programs. Also available are commands to read and punch paper tape, execute program segments, and display and alter memory locations and CPU registers. The Hardware Reference Manual supplied with the RMC-80/10 contains a source listing of the system monitor. This listing allows the user to execute existing routines by using CALL and JUMP instructions.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

D	Display Memory
G	Execute Program
I	Insert into Memory
M	Move Memory
R	Read Hexadecimal File
S	Substitute Memory
W	Write Hexadecimal File
X	Examine and Modify Registers
B	Write BNPF File

Specifications

Refer to specifications for BLC-80/10, BLC-604, and BLC-635.

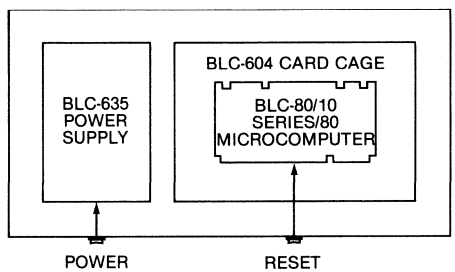
Front Panel Switches —	Power On/Off Reset		
System Monitor —	Addresses $0000-0506_{16}$ (ROM) $3C00-3C3F_{16}$ (RAM)		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
DC Power Available for Expansion Boards —	+12V, 1.6A +5V, 10.0A −5V, 0.9A −12V, 0.625A Assumes fully loaded CPU board with PROM's and terminators installed.		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	3.5 in.	(8.89 cm)
	Width	19 in.	(48.26 cm)
	Depth	20 in.	(50.8 cm)
	Weight	37 lb.	(16.8 kg)

Order Information

RMC-80/10	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/10E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/10 CPU board, BLC-635 Power Supply, BLC-910 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

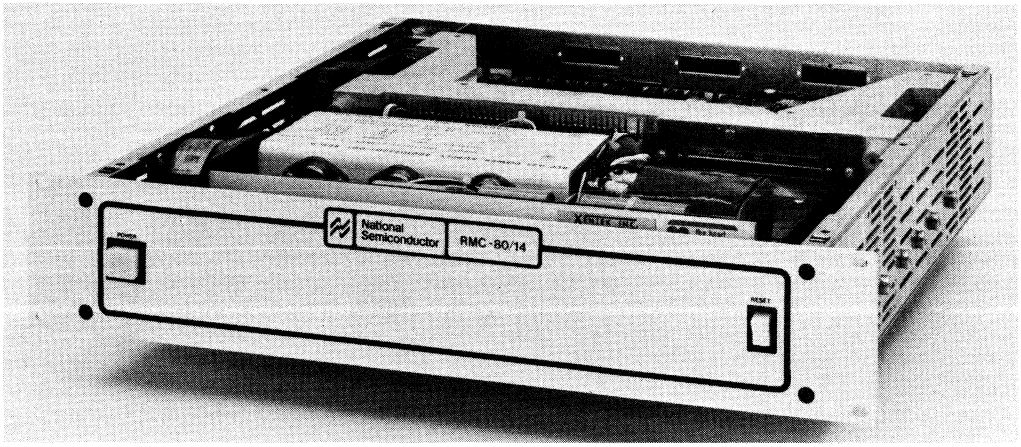
Documentation

420305535-001	RMC-80/10 Enclosure Monitor User's Manual
420305506-001	RMC-80/10 Rack Mountable Computer Hardware Reference Manual (3 manual set)
420305489-001	BLC-635 Power Supply User's Manual



RMC-80/10 Diagram

RMC-80/14
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/14 Board Level Computer
  - BLC-910 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power and Reset Switches**
- **Rear Panel with Provision for User Installed Connectors**
- **Expandable with Standard BLC/SBC Series/80 Products**

Product Overview

The RMC-80/14 is a packaged microcomputer system based on the BLC-80/14 Board Level Computer. The RMC-80/14 occupies only 3½ inches of vertical space in a standard 19-inch RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/14 CPU board plus three additional expansion boards. The chassis contains the CPU board, power supply, fans, and three expansion board slots.

The CPU board in the RMC-80/14 is based on the INS8080A LSI n-channel microprocessor. The RMC-80/14 is functionally compatible with the entire family of BLC/SBC hardware and software products.

Installed in the RMC-80/14 is a BLC-80/14 Board Level Computer including a CPU, a serial communications interface, 48 parallel I/O lines, 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. The RMC-80/14 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/14 CPU

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/14 CPU. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/14 contains 4K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending on the type of ROM installed.

Sockets are installed on the BLC-80/14 to allow user implementation of read only memory for the specific application. Up to 8K bytes of ROM can be installed in 1K or 2K increments. MM2308/MM2316E ROM's or low cost MM2708/MM2716 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending on the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O addresses assigned to the 8255 PPI's.

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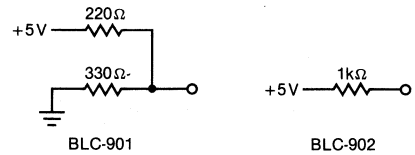
*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.



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7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. In the RS232C mode, jumper selection is available to reconfigure the port as either a data set or a data terminal. Table 2 lists the serial baud rates available.

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÷56	19.2 KHz	19200	1200	300
÷112	9.6 KHz	9600	600	150
÷224	4.8 KHz	4800	300	75
÷448	2.4 KHz	2400	150	
÷611	1.76 KHz	1760	110	

Interrupt System

The BLC-80/14 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

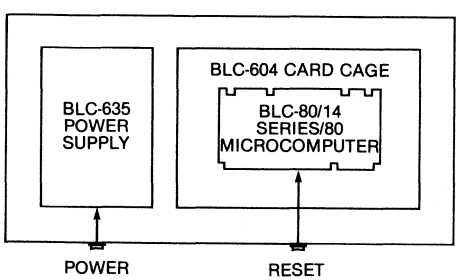
The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

BLC-910 System Monitor Firmware

Two MM2708 PROM's containing the system monitor are installed in the BLC-80/14. The monitor can be used for loading, debugging, and executing programs. Also available are commands to read and punch paper tape, execute program segments, and display and alter memory locations and CPU registers. The Hardware Reference Manual supplied with the RMC-80/14 contains a source listing of the system monitor. This listing allows the user to execute existing routines by using CALL and JUMP instructions.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

D	Display Memory
G	Execute Program
I	Insert into Memory
M	Move Memory
R	Read Hexadecimal File
S	Substitute Memory
W	Write Hexadecimal File
X	Examine and Modify Registers
B	Write BNPF File



RMC-80/14 Diagram

Specifications

Refer to specifications for BLC-80/14, BLC-604, and BLC-635.

Front Panel Switches —	Power On/Off Reset		
System Monitor —	Addresses $0000-0506_{16}$ (ROM) $3C00-3C3F_{16}$ (RAM)		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
DC Power Available for Expansion Boards —	+12V, 1.6A +5V, 10.0A −5V, 0.9A −12V, 0.625A Assumes fully loaded CPU board with PROM's and terminators installed.		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height Width Depth Weight	3.5 in. 19 in. 20 in. 37 lb.	(8.89 cm) (48.26 cm) (50.8 cm) (16.8 kg)

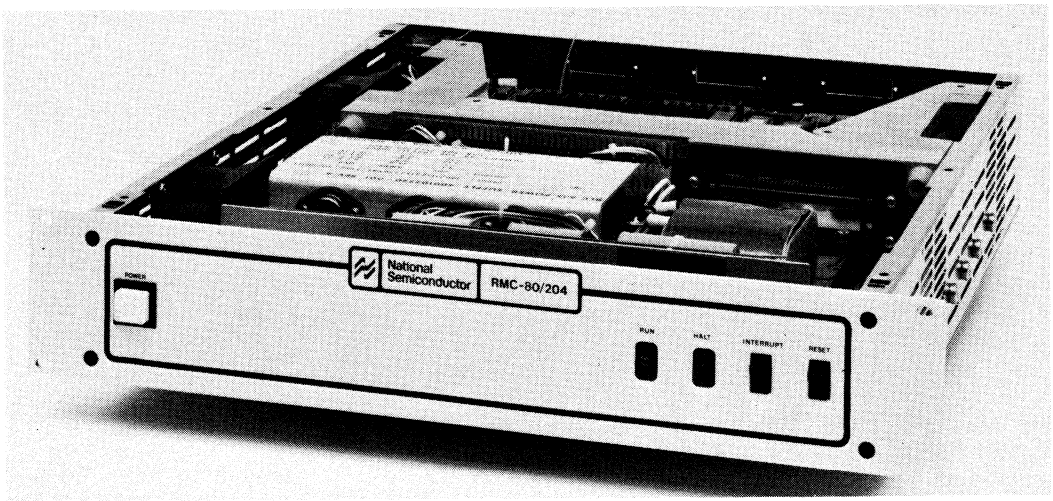
Order Information

RMC-80/14	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/14E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/14 CPU board, BLC-635 Power Supply, BLC-604 Card Cage, BLC-910 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

Documentation

420305620-001	RMC-80/14 Enclosure Monitor User's Manual
420305489-001	BLC-635 Power Supply User's Manual
420305506-002	RMC-80/14 Rack Mountable Computer Hardware Reference Manual (3-manual set)

RMC-80/204
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/204 Board Level Computer
  - BLC-920 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power, Reset, and Interrupt Switches and Halt and Run Status Indicators**
- **Rear Panel with Provision for User Installed Connectors**
- **Expandable with Standard BLC/SBC Series/80 Products**
- **Replacement for Intel's System 80/20 and System 80/20-4**

Product Overview

The RMC-80/204 is a packaged OEM microcomputer system based on the BLC-80/204 Board Level Computer. The RMC-80/204 occupies only 3½ inches of vertical space in a standard RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/204 CPU board plus three additional expansion boards. The chassis contains the CPU board, power supply, dual fans, and three expansion slots.

The RMC-80/204 may be expanded beyond the basic system through additional CPU boards, RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/204 CPU

The BLC-80/204 is a self-contained board level computer including the central processor, system clock, RAM and PROM memories, 48 I/O lines, an RS232C serial communications interface, hardware vectored interrupt logic, multiprocessor bus arbitration capability, three programmable timers, and bus logic and drivers.

The INS8080A-2 n-channel LSI microprocessor is the central processor for the BLC-80/204. The INS8080A-2 provides six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly or in pairs when double precision operations are required. The 16-bit program counter allows direct

addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the 64K memory space. The stack may be used to store the contents of the various registers while interrupts and subroutines are being services.

4K bytes of static read/write memory are provided by MM5257 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations on the CPU board are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/204 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and is cabled to the power supply.

BLC-635 Power Supply

The self-contained BLC-635 Power Supply is designed to power the CPU board and three additional expansion boards. Overvoltage and overcurrent protection is provided, and an AC Low signal is generated under low line conditions.

BLC-920 System Monitor Firmware

The system monitor is supplied with the RMC-80/204 in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register.

The system monitor also permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I	Insert into memory
X	Examine and modify CPU register
S	Substitute memory
M	Move memory
D	Display memory contents and addresses
A	Display memory contents in hex and ASCII
F	Display memory contents for search value
H	Display sum and difference
O	Write output byte
W	Write hexadecimal file
R	Read hexadecimal file
T	Display input port contents
G	Go execute program
N	Single step (next instruction)

Specifications

Refer to specifications for BLC-80/204, BLC-604, and BLC-635.

Front Panel

Switches —	Power On/Off Reset Interrupt
Indicators —	Halt Run
System Monitor —	Addresses 0000-069C$_{16}$ (ROM) 3F80-3FFF$_{16}$ (RAM)
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz
DC Power Available for Expansion Boards —	+12V, 1.65A +5V, 9.1A −5V, 0.7A −12V, 0.8A Assumes fully loaded CPU board with PROM's and terminators installed.
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

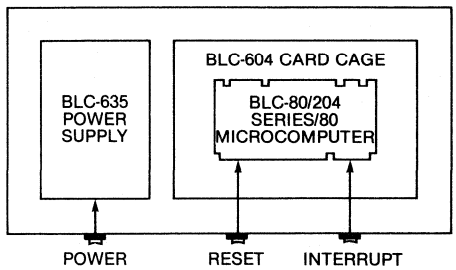
Physical —			
	Height	3.5 in.	(8.89 cm)
	Width	19 in.	(48.26 cm)
	Depth	20 in.	(50.8 cm)
	Weight	37 lb.	(16.8 kg)

Order Information

RMC-80/204	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/204E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/204 CPU board, BLC-635 Power Supply, BLC-604 Card Cage, BLC-920 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

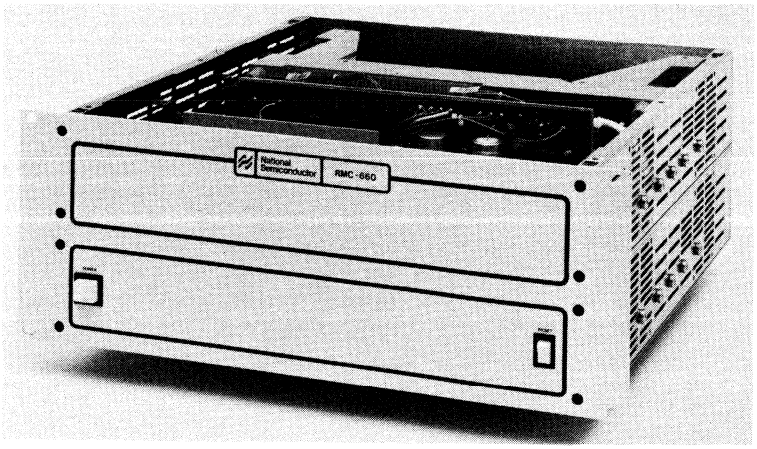
Documentation

420305761-001	RMC-80/204 Enclosure Monitor User's Manual
420305883-001	RMC-80/204 System Package (3 manual set)
420305745-001	BLC-80P204 Prototyping Package User's Manual
420305489-001	BLC-635 Power Supply User's Manual



RMC-80/204 Diagram

RMC-660
System Chassis



- **Allows Large OEM Configuration of Series/80 Products**
  - 8-slot card cage
  - Heavy duty 30 Amp power supply
- **Front Panel with Power and Reset Switches for Control**
- **Rear Panel Accepts a Variety of User Connectors**
- **Plug-replacement for SBC-660 System Chassis**

Product Overview

The RMC-660 System Chassis supports Series/80 Board Level Computers and the full complement of expansion boards. The chassis occupies 7 inches of vertical rack space in a standard 19-inch RETMA rack. The System Chassis includes a BLC-665 Heavy Duty Power Supply, cooling fans, and an 8-slot card cage including a printed circuit board bus.

Functional Description

The BLC-665 Heavy Duty Power Supply provides regulated DC outputs of ±5 and ±12 volts. Current limiting and overvoltage protection is provided on all outputs. Logic provided in the power supply senses an AC power failure or low line condition and generates a TTL compatible signal for an orderly system shutdown sequence. The power supply is connected to the 8-slot card cage by a mating cable set.

The front panel contains a power on-off switch and a reset switch which connects to the system bus of a CPU for external system control.

The RMC-660 is ideal for OEM applications requiring up to 8 boards.

Specifications

Refer to detailed specifications for BLC-665 Heavy Duty Power Supply.

Front Panel Switches —	Power On/Off Reset		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	7.00 in.	(17.8 cm)
	Width	19.00 in.	(48.3 cm)
	Depth	20.00 in.	(50.8 cm)
	Weight	49 lb.	(22.2 kg)

Order Information

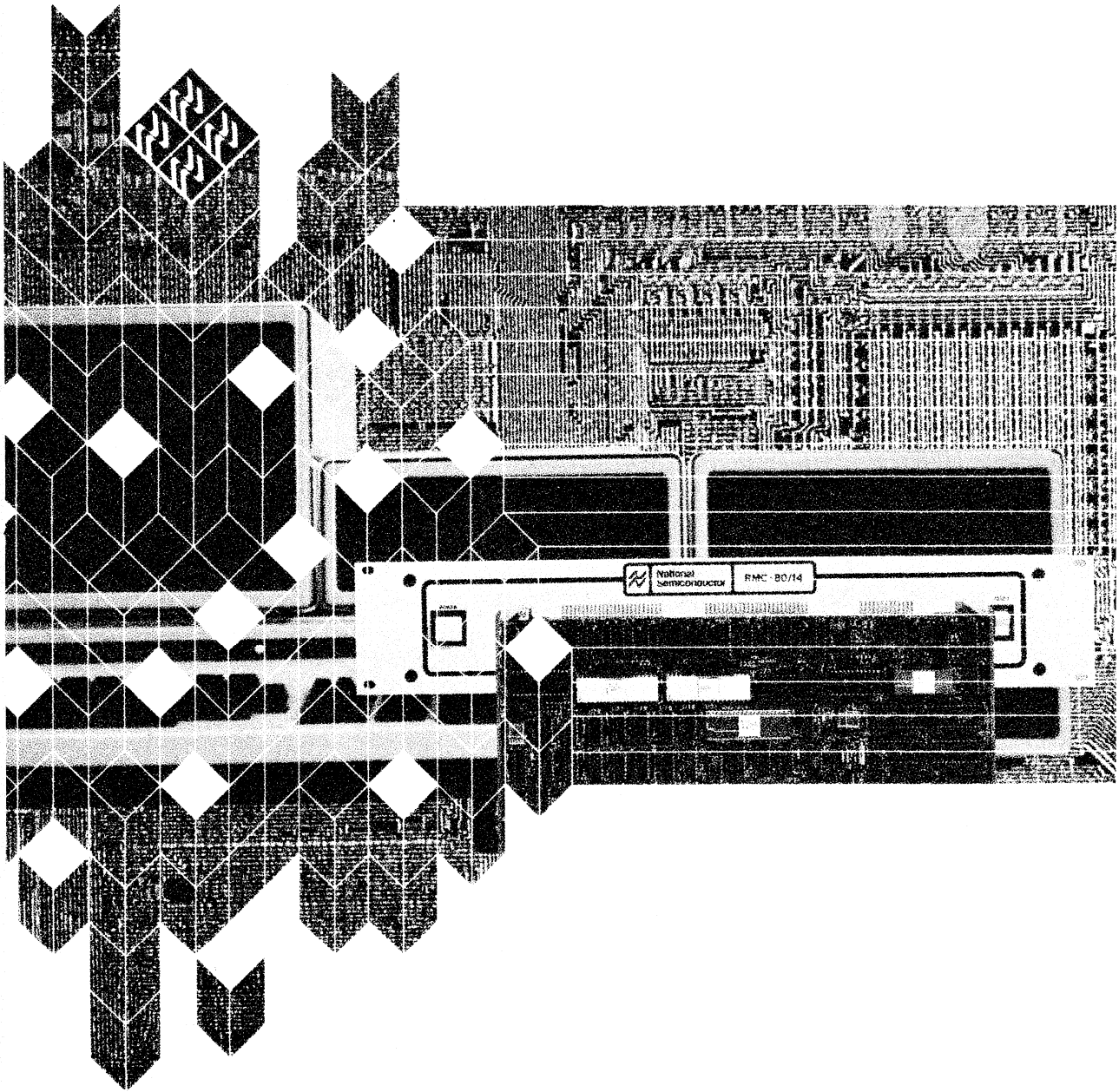
RMC-660	System Chassis, 110-115 VAC, 60 Hz.
RMC-660E	System Chassis, 200-230 VAC, 50 Hz.

Both systems include: card cage and backplane assembly, BLC-665 Heavy Duty Power Supply, 115 volt power cable, 115 volt and 230 volt fuses, 8-slot card cage, dual fans, backplane schematic drawing, RMC-660 assembly drawings and documentation.

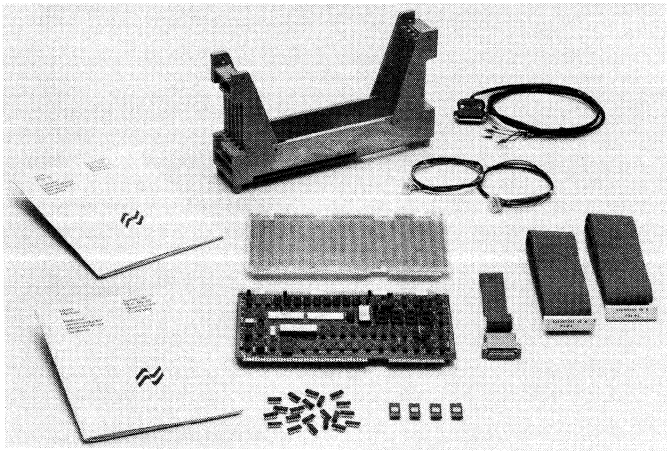
Documentation

420305561-001	RMC-660 Enclosure User's Manual
420302220-001	BLC-665 Power Supply User's Manual

Section 3
Prototyping Systems



BLC-80P
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
  - BLC-80/10 CPU
  - Universal Prototyping Board
  - Card Cage
  - EPROM
- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables

Product Overview

The BLC-80P Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/10 CPU board with a BLC-910 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/10 CPU

The BLC-80/10 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, I/O lines, serial communications interface, and bus logic and drivers.

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The 8080A provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly, or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory, which may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

1K bytes of static read/write memory are provided by 8 MM2111 RAM's while sockets for MM2708 EPROM's provide up to 4K bytes of read only memory in 1K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/10 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-910 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Programs may be loaded from or saved on paper tape by using an appropriate teletypewriter device and selecting the teletypewriter jumper options on the CPU board.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory

W — Write hexadecimal file

R — Read hexadecimal file

B — Write BNPF file

G — Go execute program

Accessories

The BLC-80P Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/10 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/10 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)

Specifications

Refer to Specifications for BLC-80/10, BLC-8905 and BLC-604.

Power — +5V, 2.9A
−5V, 0.02A
+12V, 0.05A
−12V, 0.15A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

Height	8.5 in.	(21.59 cm)
Width	14.2 in.	(36.07 cm)
Depth	3.34 in.	(8.48 cm)
Weight	3.4 lbs.	(1.5 kg)

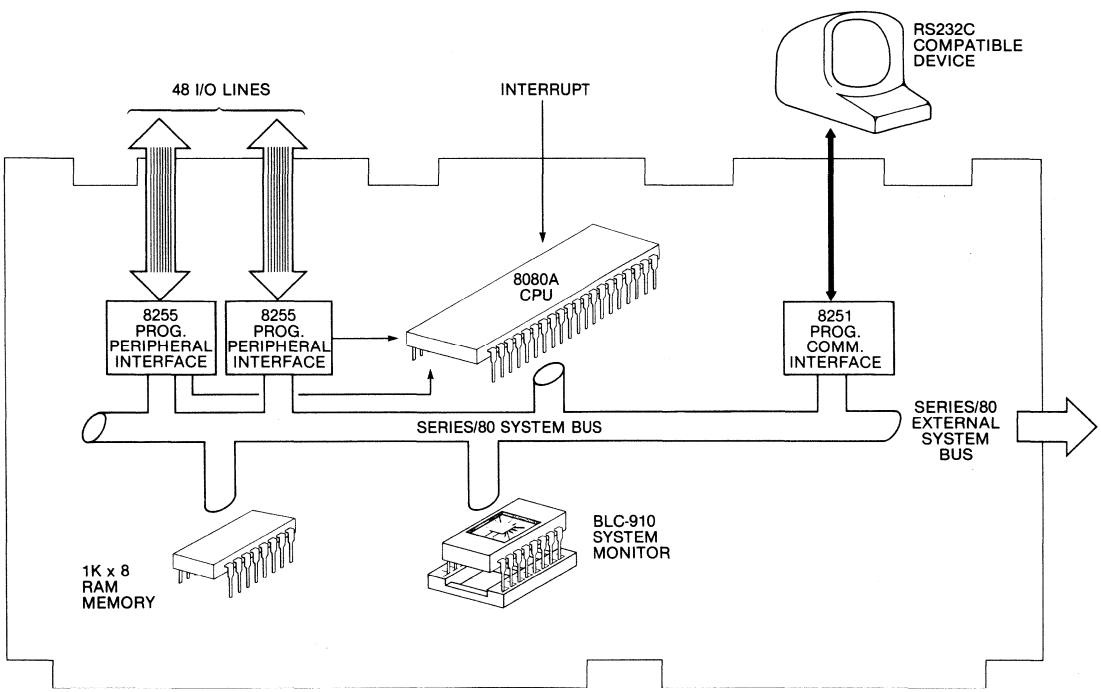
Order Information

BLC-80P — Prototyping Package with a BLC-80/10 Board Level Computer including 1K bytes of static RAM and sockets for 2K bytes of EPROM. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers and cables.

Documentation

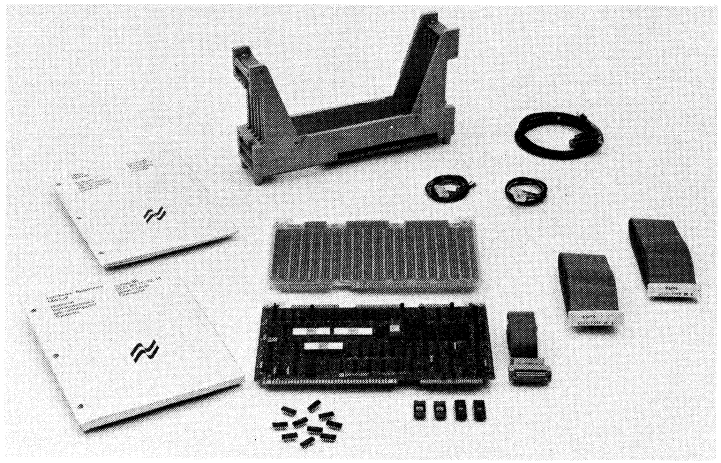
420305521-001 BLC-80P Prototyping Package User's Manual.

420305373-001 BLC-80/10 Board Level Computer Hardware Reference Manual.



BLC-80P Diagram

BLC-80P14
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
  - BLC-80/14 CPU
  - Universal Prototyping Board
  - Card Cage
  - EPROM
- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables

Product Overview

The BLC-80P14 Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/14 CPU board with a BLC-910 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P14 contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P14 is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/14 CPU

The BLC-80/14 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, I/O lines, serial communications interface, and bus logic and drivers.

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/14. The 8080A provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly, or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory. The stack may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

4K bytes of static read/write memory are provided by MM2114 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/14 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-910 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Programs may be loaded from or saved on paper tape by using an appropriate teletypewriter device and selecting the teletypewriter jumper options on the CPU board.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory

W — Write hexadecimal file

R — Read hexadecimal file

B — Write BNPF file

G — Go execute program

Accessories

The BLC-80P14 Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- Ten DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/14 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/14 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)

Specifications

Refer to Specifications for BLC-80/14, BLC-8905 and BLC-604.

Power — +5V, 2.9A
−5V, 0.02A
+12V, 0.05A
−12V, 0.15A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

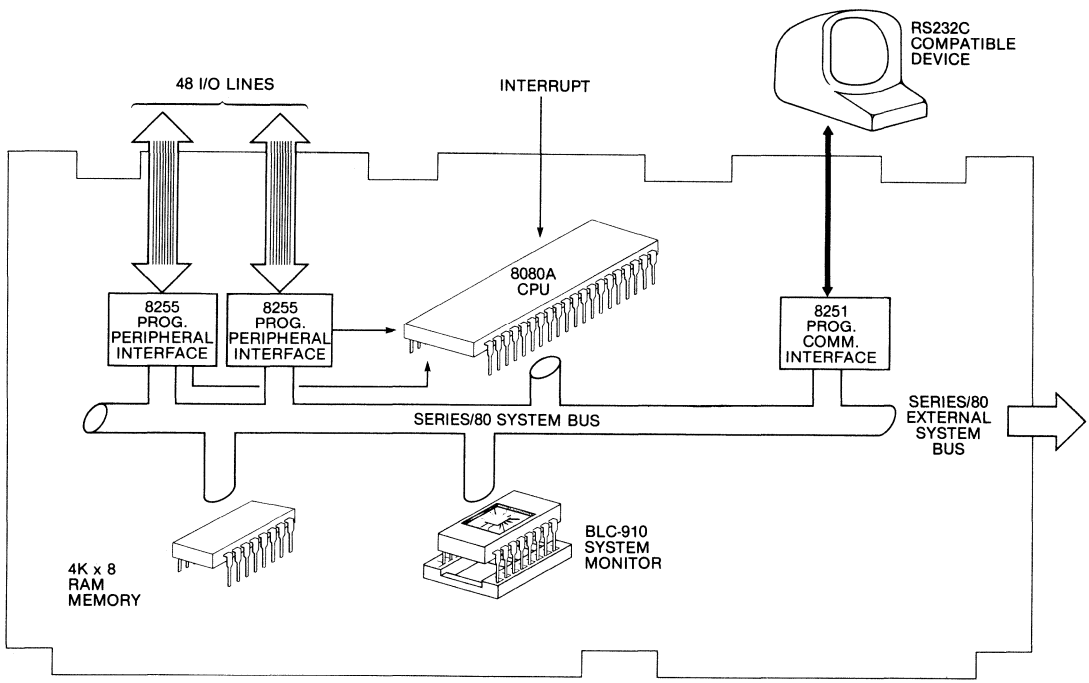
Height	8.5 in.	(21.59 cm)
Width	14.2 in.	(36.07 cm)
Depth	3.34 in.	(8.48 cm)
Weight	3.4 lbs.	(1.5 kg)

Order Information

BLC-80P14	Prototyping Package with a BLC-80/14 Board Level Computer including 4K bytes of static RAM and sockets for up to 8K bytes of EPROM. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers and cables.

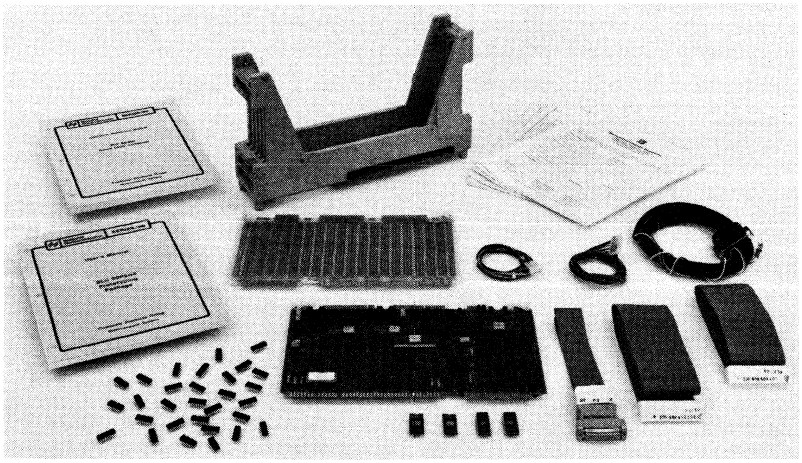
Documentation

420305618-001	BLC-80P14 Prototyping Package User's Manual.
420305532-001	BLC-80/11, 80/12, 80/14 Board Level Computer Hardware Reference Manual.



BLC-80P14 Diagram

BLC-80P204
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
  - BLC-80/204 CPU
  - Universal Prototyping Board
  - Card Cage
  - EPROM
- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables
  - Current Loop Adapter

Product Overview

The BLC-80P204 Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/204 CPU board with a BLC-920 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P204 contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P204 is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/204 CPU

The BLC-80/204 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, 48 I/O lines, an RS232C serial communications interface, hardware vectored interrupt logic, multiprocessor bus arbitration capability, three programmable timers, and bus logic and drivers.

The INS8080A-2 n-channel LSI microprocessor is the central processor for the BLC-80/204. The 8080A-2 provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory. The stack may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

4K bytes of static read/write memory are provided by MM5257 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/204 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-920 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory contents and address

A — Display memory contents

F — Display memory contents for search value

H — Display sum and difference

O — Write output byte

W — Write hexadecimal file

R — Read hexadecimal file

T — Display input port contents

G — Go execute program

N — Single step (next instruction)

Accessories

The BLC-80P204 Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- Ten DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/204 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/204 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)
- One BLC-530 Current Loop Adapter

Specifications

Refer to Specifications for BLC-80/204, BLC-8905 and BLC-604.

Power — +5V, 4.9A
−5V, 0.18A
+12V, 0.35A
−12V, 0.02A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%, non-condensing

Physical —			
	Height	8.5 in.	(21.59 cm)
	Width	14.2 in.	(36.07 cm)
	Depth	3.34 in.	(8.48 cm)
	Weight	4 lbs.	(1.8 kg)

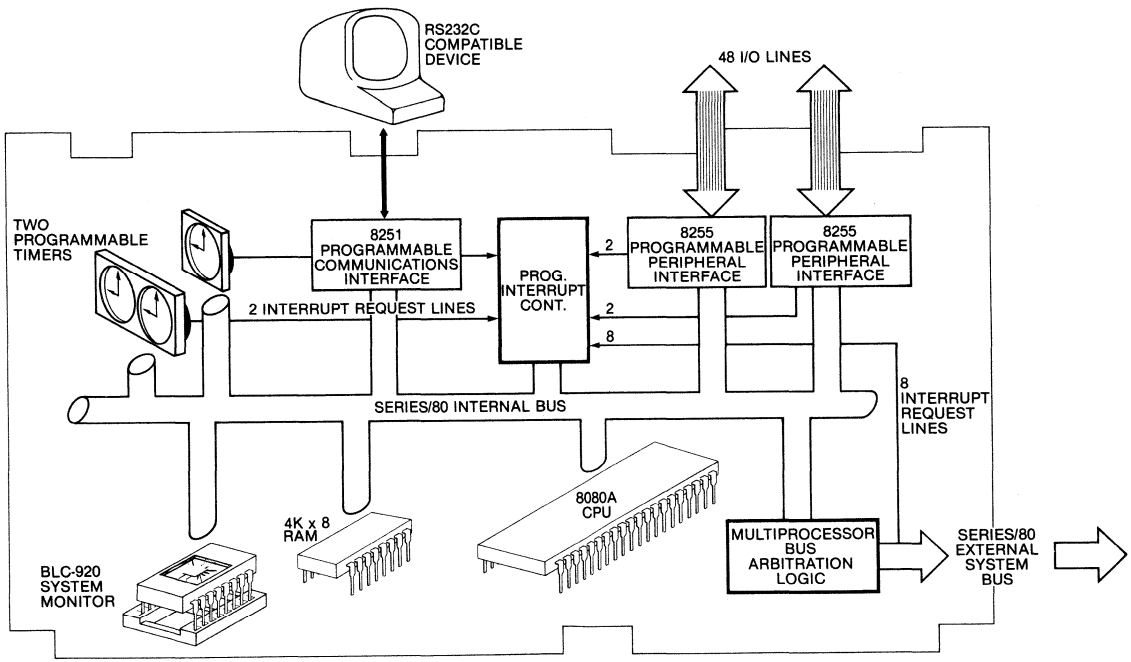
Order Information

BLC-80P204 Prototyping Package with a BLC-80/204 Board Level Computer including 4K bytes of static RAM and sockets for 4K bytes of EPROM using MM2708 modules or 8K bytes of EPROM using MM2716 modules. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers, cables, and current loop adapter.

Documentation

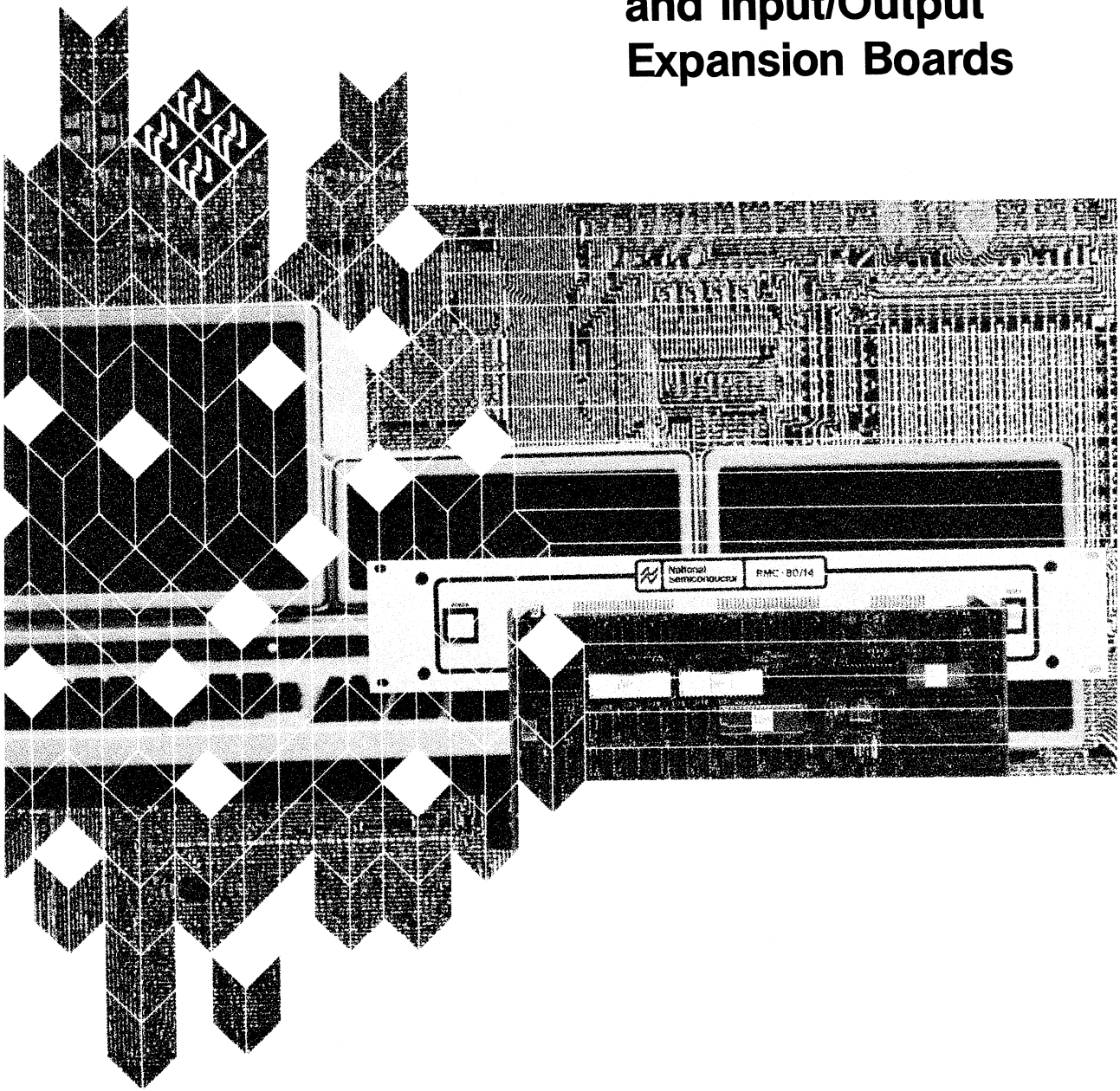
420305745-001 BLC-80P204 Prototyping Package User's Manual.

420305521-001 BLC-80/204 Board Level Computer Hardware Reference Manual.



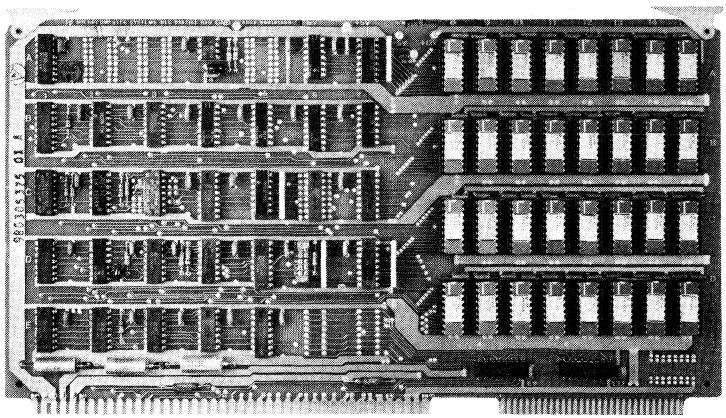
BLC-80P204 Diagram

Section 4
Memory and Combination Memory and Input/Output Expansion Boards



National Semiconductor

BLC-016
RAM Memory Board



- **Flexible System Implementation**
  - User-selectable starting address
  - 16K to 64K bytes in a single Series/80 system
- **On-board Refresh Eliminates the Need for a Separate Control Board**
- **Ease of Maintenance**
  - Socketed MM5271 4K x 1 dynamic RAM's
  - Address selection using BERG™ jumpers
- **Fully Compatible with BLC/SBC Products**
  - Plug-replacement for Intel's SBC-016

Product Overview

The BLC-016 is a member of a family of Series/80 memory and I/O expansion boards available from National Semiconductor. Compatible with all National Series/80 CPU boards, the BLC-016 plugs directly into any Series/80 card cage or system.

Flexible design allows selection of memory starting addresses to suit the system configuration. This is especially important when using a mix of memory increments or memory board capacities.

Functional Description

Based on National's MM5271 dynamic 4K x 1 RAM, the BLC-016 includes read/write data buffers, TTL compatible data, address and command lines, and on-board refresh logic.

On-board refresh of the entire 16K bytes of RAM is accomplished every two milliseconds. Each refresh cycle takes 700 nanoseconds, with a 64-bit block in each of the 32 MM5271 dynamic RAM's refreshed every 29 microseconds. System stability is maintained by inhibiting refresh when a read or write cycle is in progress.

High impedance TRI-STATE™ buffers are employed where address, data and command functions interface with the Series/80 system bus.

Address selection is implemented in contiguous 16K byte blocks beginning at memory locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$. Memory addresses used by the CPU on-board RAM and ROM are not available to the BLC-016 except for CPU's containing on-board RAM/ROM disable capability. Address blocks are easily selected using BERG™ jumper plugs.

Up to four BLC-016 RAM boards or a total of 64K bytes may be used in a single Series/80 system.

The array of 32 MM5271 RAM's is socketed for ease of troubleshooting, repair and maintenance of the BLC-016 board. Spare components may be inventoried rather than entire boards.

Specifications

Memory Size —	16K bytes
Word Size —	8 bits
Cycle Times —	Read — 700 ns Write — 1160 ns Refresh — 700 ns
Address Selection —	Jumper selection of contiguous 16K byte blocks starting at locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
System Bus Connector —	86 contact double-sided card cage edge connector on 0.156 inch centers
Power —	+5V, 1.5A −5V, 0.01A +12V, 0.7A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

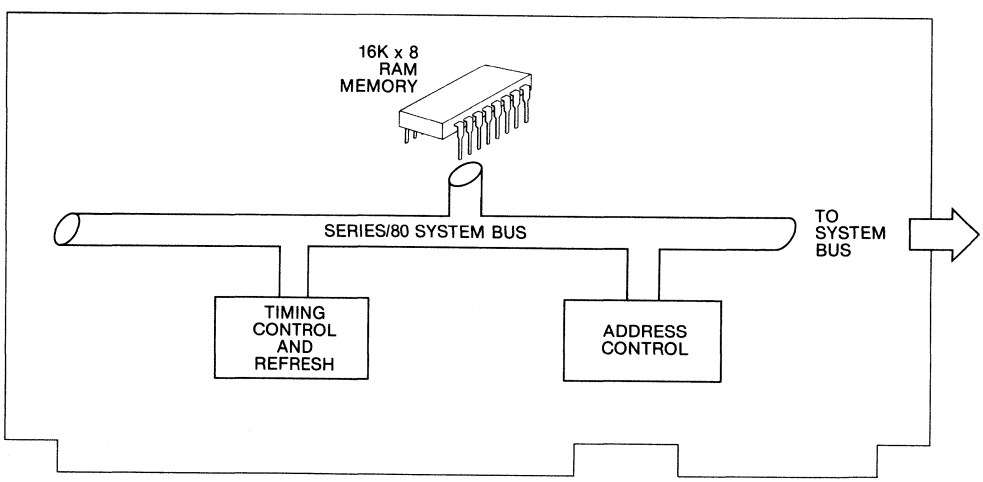
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-016	16K Byte RAM Board

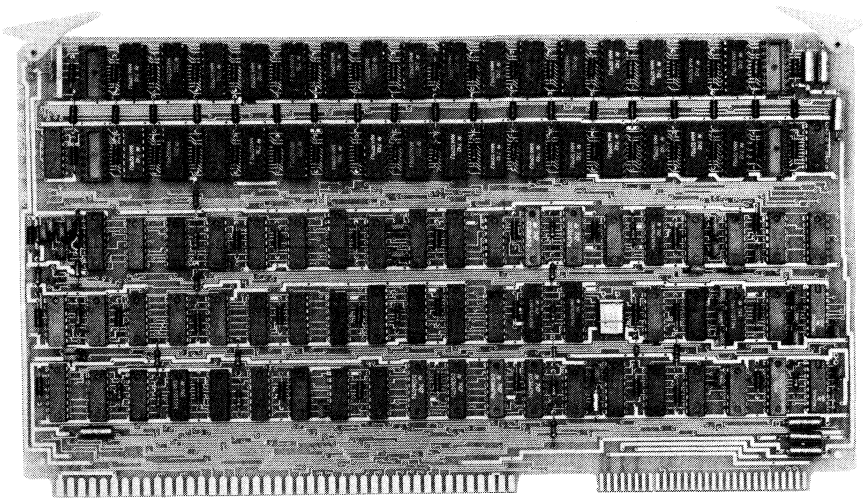
Documentation

420305375-001	BLC-016 16K Byte RAM Board User's Manual.



BLC-016 Diagram

BLC-8016, BLC-032, BLC-048, and BLC-064 Ram Memory Boards



- **Flexible System Configuration**
  - BLC-8016 — 16K bytes
  - BLC-032 — 32K bytes
  - BLC-048 — 48K bytes
  - BLC-064 — 64K bytes
  - 8- or 16-bit data access
- **Enhanced System Performance**
  - On-board refresh and control logic
  - Synchronized (transparent) refresh capability — no refresh wait state with BLC-80/204
  - Auxiliary power bus and memory protect logic for battery backup requirements
- **Ease of Maintenance**
  - Socketed MM5290 16K × 1 and MM5298 8K × 1 dynamic RAMs
- **Fully Compatible with BLC/SBC Products**
  - Plug-replacements for BLC-016 and SBC-016/032/048/064

Product Overview

The BLC-8016, BLC-032, BLC-048 and BLC-064 RAM expansion boards are designed to meet large memory requirements without sacrificing space or significantly reducing available power. These boards provide 16K bytes, 32K bytes, 48K bytes and 64K bytes, respectively, of dynamic random access read/write memory (RAM) on a single printed circuit board. The boards are complete with all refresh and control electronics, address and data buffers, and memory array.

Designed-in flexibility permits the user to obtain the optimum system configuration. Starting address segments are provided at 16K byte boundaries and data may be accessed in 8- or 16-bit modes. Memory may be expanded up to one megabyte in a single Series/80 system by using the BLC-064 and implementing logic to activate additional, existing address lines.

The BLC-8016, BLC-032, BLC-048 and BLC-064 are plug-compatible replacements for Intel's SBC-016, 032, 048 and 064 and BLC-016, and plug directly into any BLC/SBC system.

Functional Description

The BLC-8016, -032, -048 and -064 are based on National's MM5290 16K × 1-bit and MM5298 8K × 1-bit dynamic RAM modules. Memory access time is a fast 430 nanoseconds and a full read or write cycle takes only 660 nanoseconds. The

memory complement is organized into independent 16K × 8-bit address blocks. Each block may be configured to a unique starting address on one of four 16K byte boundaries. In the case of the BLC-8016, BLC-032 and BLC-048 this allows the user greater flexibility when using other Series/80 System ROM/PROM memory or I/O boards.

The board can be used in an eight or sixteen bit data mode. A separate control signal on the Series/80 system bus provides data mode selection under system control.

The BLC-8016, -032, -048 and -064 have a 20-bit address bus. This permits the sophisticated user to combine up to 16 BLC-064 RAM boards to create a megabyte memory system. Normally, 8080 based systems use only 16 of the 20 available address bits; however, board select logic may be enabled to allow a BLC-064 to occupy any one of sixteen 64K byte blocks within a megabyte address range.

Synchronized Refresh

On-board automatic refresh logic is used to refresh a portion of the total memory every 13 microseconds. Refresh logic waits for an in-process memory access cycle to be completed before initiating a refresh cycle. In addition there is a special status signal implemented on the BLC-80/204 microcomputer for refresh synchronization. When enable, this feature causes BLC-8016, -032, -048 and -064 memory refresh cycles to synchronize with CPU activity and results in increased system throughput and consistent software timing loop results.

Memory Protect

Memory protection of RAM contents is provided through an auxiliary connector on the memory board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This input is provided for the protection of RAM contents during a system power-down sequence.

Specifications

Memory Size —	BLC-8016 — 16K bytes BLC-032 — 32K bytes BLC-048 — 48K bytes BLC-064 — 64K bytes
Word Size —	8 or 16 bits
Access Time —	430 ns
Cycle Times —	Read — 660 ns Write — 660 ns (delayed write) 1230 ns (advanced write) Refresh — 615 ns
Address Selection —	Jumper selection of contiguous 16K byte blocks starting at locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$
System Bus Connector —	Data, address and command signals are TRI-STATE™ TTL compatible
System Bus Connector —	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary Power —	Separate power bus provided for systems requiring battery backup of memory for critical applications. On-board jumpers provided to enable this mode of operation.
Power —	(BLC-048 and BLC-064)

	Operating	Battery
+5V	3.0A	1.7A
−5V	0.011A	0.011A
+12V	0.47A	0.140A

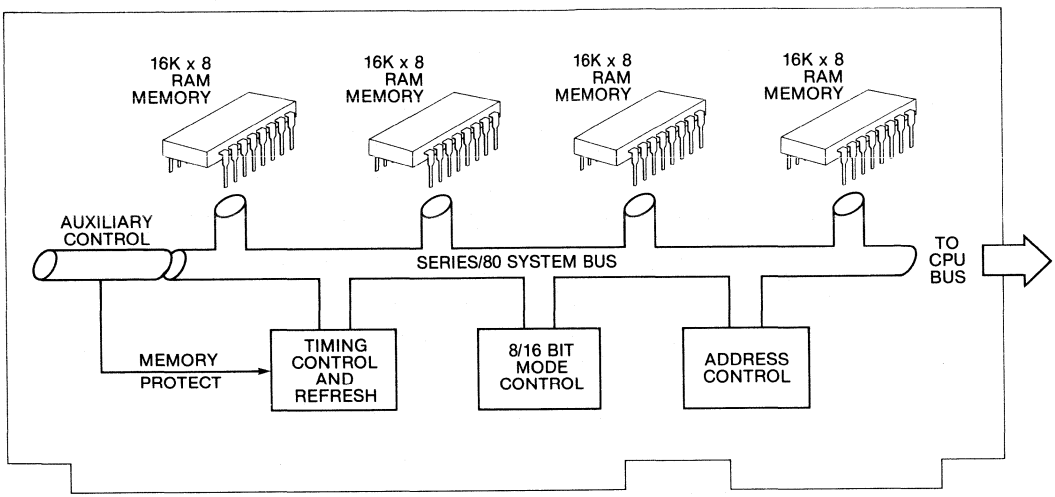
Environmental —	Temperature 0 °C to 55 °C	
	Humidity 0 to 90% non-condensing	
Physical —	Height 6.75 in.	(17.15 cm)
	Width 12.00 in.	(30.48 cm)
	Depth 0.50 in.	(1.27 cm)
	Weight 14 oz.	(396.9 g)

Order Information

BLC-8016	16K Byte RAM board
BLC-032	32K Byte RAM board
BLC-048	48K Byte RAM board
BLC-064	64K Byte RAM board

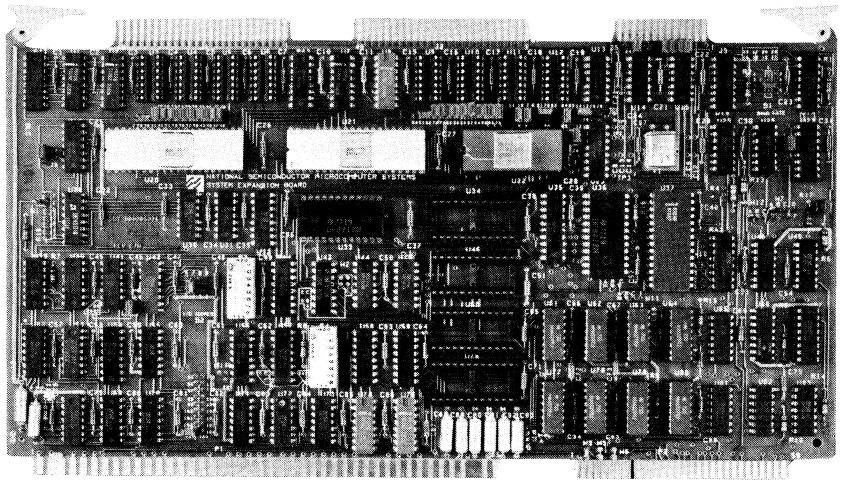
Documentation

420305529-001	BLC-8016/032/048/064, 16K/32K/48K/64K Byte RAM Board Hardware Reference Manual



BLC-064 System Diagram

BLC-104 and BLC-116 Memory and Input/Output Boards



- **Flexible Memory Combinations**
  - 4K RAM and up to 8K PROM
  - 16K RAM and up to 8K PROM
  - 4K byte address boundaries
  - ROM can be implemented in 1K segments
- **Battery Back-Up Logic for System Memory Integrity**
- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal with Baud Rates of 75 to 38.4K**
- **8 Maskable Interrupts and 1 millisecond Timer Permit Easy System Control**
- **Plug-replacements for SBC-104 and SBC-116**

Product Overview

The BLC-104 and BLC-116 Memory and Input/Output Expansion Boards provide a combination of memory and digital input/output capability ideally suited to smaller system applications where space and system optimization are critical.

Memory is provided for both read/write and read only requirements. The BLC-104 contains 4K bytes of dynamic RAM and sockets for up to 8K bytes of PROM while the BLC-116 contains 16K bytes of dynamic RAM and sockets for up to 8K bytes of PROM. ROM/PROM is implemented using MM2308/MM2316E ROM modules or MM2708/MM2716 PROM modules.

Both parallel and serial input/output are provided — 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-104 and BLC-116 are plug-replacements for Intel's SBC-104 and SBC-116 boards.

Functional Description

Read/Write Memory

The BLC-104 read/write RAM is based on National's MM4027 4K x 1-bit dynamic RAM modules; the BLC-116 uses MM4116 16K x 1-bit dynamic RAM modules. RAM modules are socket mounted for fast troubleshooting and repair. Memory access time is 575 nanoseconds and a full read or write cycle takes only 665 nanoseconds. Memory refresh is asynchronous and independent of the CPU. RAM addressing is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Memory contents may be protected by using an auxiliary connector on the board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This feature protects RAM contents during a system power-down sequence and permits the battery back-up to maintain the memory refresh function.

Read Only Memory

The ROM section is designed to accept MM2708/MM2716 Programmable Read Only Memory (PROM) or MM2308/MM2316E ROM modules. While four sockets are provided for the maximum configuration, only the number of PROM modules required for the application are necessary. ROM access time is a fast 465 nanoseconds with a maximum full cycle time of 685 nanoseconds.

The ROM section address is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in bidirectional modes. The parallel input/output section is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.
- Data read or write to the specified port using strobe or handshake signals created by or transmitted to the interfaced external device.
- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B. Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line drivers and terminators circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

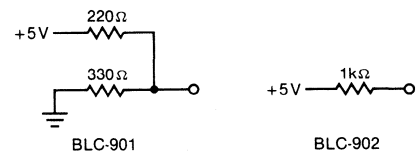


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps (see Table I).

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial Input/Output

The serial I/O port control is based on a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and

contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4800
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect parity. Figure 2 illustrates the status word.

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-104 and BLC-116 are designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

I/O Section Addressing

The input/output section uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

7	6	5	4	3	2	1	0
Data Set Ready	SYNC Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

Specifications

RAM Memory

Memory Size — BLC-104 — 4K bytes
BLC-116 — 16K bytes

Word Size — 8 bits

Access Time — 575 ns

Cycle Time — Read 665 ns
Write 665 ns
Refresh Delay 405 ns

Address Select — Switch and jumper selection
4K byte boundaries

ROM Memory

Memory Size — 8K bytes (PROM)

Word Size — 8 bits

Access Time — 465 ns

Address Select — Switch and jumper selection
4K byte boundaries

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7408	I, OC	16
7403	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting;
OC = open collector;
HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Character Length — 5-, 6-, 7- or 8-bit

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous)

75	1200
110	2400
150	4800
300	9600
600	19200

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer — 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M "Schotchflex" 3463-001

Parallel I/O — 50 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-001
AMP 2-86792-3
Recommended cables:
BLC-956 Parallel I/O Cable Kit
(two 5 foot ribbon cables)

Serial I/O	26 contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-0001 flat AMP 1-583715-1 round

Power

	BLC-104	BLC-116	Battery
+5V	4.1 A	4.6 A	0.9 A
−5V	0.19 A	0.19 A	0.002 A
+12V	0.65 A	0.65 A	0.3 A
−12V	0.05 A	0.05 A	—

(Assumes ROM and I/O drivers installed.)

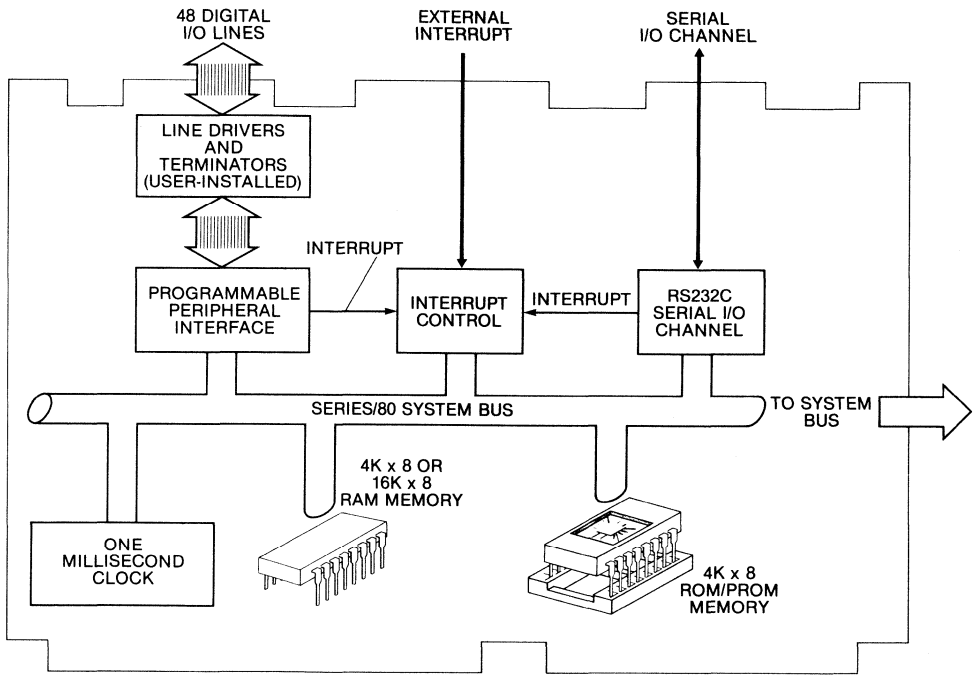
Environmental	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.0 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-104	RAM, ROM and I/O Expansion Board. Contains 4K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines and 1 millisecond interval clock.
BLC-116	RAM, ROM and I/O Expansion Board. Contains 16K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines, and a 1 millisecond interval clock.

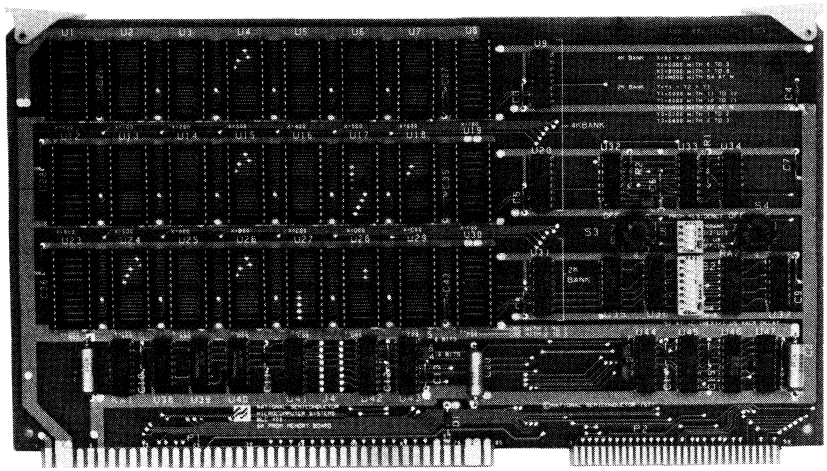
Documentation

420305376-001	BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual.



BLC-104 and BLC-116 Diagram

BLC-406
6K Byte Read Only Memory Board



- **6K Bytes of Non-Volatile ROM/PROM Storage for Firmware Programs**
- **2K and 4K Banks Provide Flexibility**
  - 8- or 16-bit Memory Word Size
- **Switch Select Memory Addressing for Easy System Integration**
- **Variable Access Time for a Variety of 1702 PROM's**
- **Plug-replacement for SBC-406**

Product Overview

The BLC-406 6K byte Read Only Memory Board is designed for use in applications requiring non-volatile fixed programs (firmware). The BLC-406 extends any BLC/SBC microcomputer's on-board read only memory, leaving the on-board RAM available for scratch pad or transient operations.

A completely populated BLC-406 board requires 24 modules using National's MM1702A or MM1302 PROM/ROM type circuits. Sockets for the modules are provided on the board.

The BLC-406 is a plug-replacement for Intel's SBC-406.

Functional Description

The BLC-406 is organized in two read only sections, a 4K byte array and a 2K byte array. Up to 24 MM1702A Programmable Read Only Memory (PROM) or MM1302 Read Only Memory (ROM) modules may be installed. A 2K byte array requires 8 ROM/PROM modules while a 4K byte array requires 16.

Access time is a function of the particular ROM/PROM modules used and ranges between 1 and 2.5 microseconds. Timing control circuits on the BLC-406 permit synchronization with the particular ROM/PROM timing characteristics.

The 8-bit byte memory word length may be changed to a 16-bit word length using on-board jumpers. 2K words are available when the BLC-406 is used as a 16-bit word memory.

On-board switches allow user selection of address assignment. The 4K and 2K byte address blocks may be independent or double assigned for a 16-bit word configuration. Addresses may be assigned on any 2K byte boundary within the 64K byte system address range.

Specifications

Memory Size —	6K bytes (8-bit) 2K words (16-bit)
Word Size —	8 or 16 bits
Access Time —	Variable, 1 to 2.5 microseconds
Address Selection —	Jumper selection of contiguous 2K byte blocks
System Bus Interface —	All address, data and control signals are TRI-STATE™ compatible
System Bus Connection —	86 contact double-sided card cage edge connector on 0.156 inch centers
Compatible Memory Modules —	MM1302 ROM MM1742 ROM MM1702 PROM
Power —	+5V, 2.5A −10V, 1.45A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing

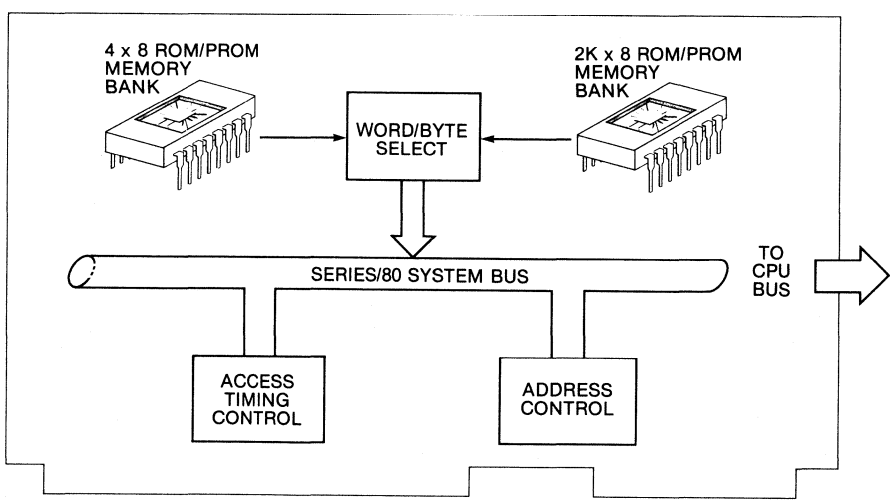
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-406	6K Byte Read Only Memory Board contains sockets for independent 4K and 2K byte banks of ROM/PROM modules

Documentation

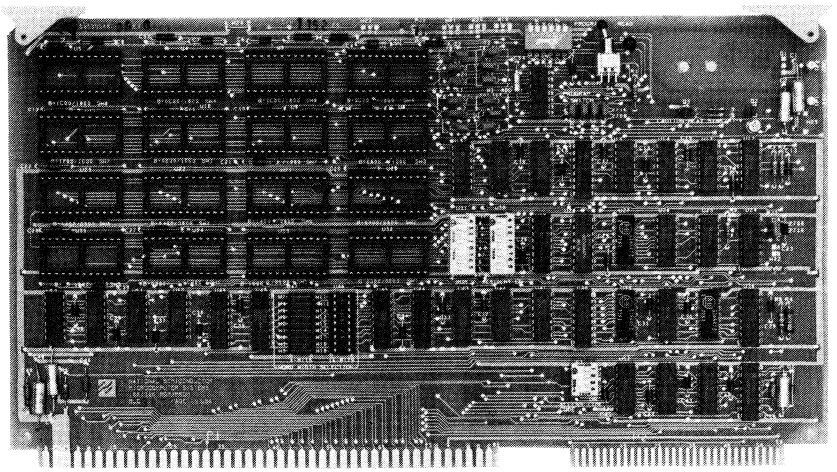
420305374-001	BLC-406 6K Byte ROM Board Hardware Reference Manual.



BLC-406 Diagram

National Semiconductor

BLC-416 and BLC-8432 16K and 32K ROM/PROM Boards



- **Complete System Flexibility**
  - Jumper options select MM2308/2708 or MM2316E/2716 devices, allowing twice the standard memory capacity
  - Selectable base addressing for independent 4K/8K blocks
  - Individual 1K/2K block enable/disable
  - On-board programming for MM2716 devices
  - Space for −5V regulator
- **Ease of Use**
  - Buffered address and data lines
  - Fully TTL compatible
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
  - Plug-replacement for SBC-416

Product Overview

The BLC-416 and BLC-8432 ROM/PROM Boards provide highly flexible, low cost, read only memory expansion for Series/80 Board Level Computers. The fully expanded board may contain 16K or 32K bytes of ROM or EPROM depending on the modules installed. The BLC-416 and BLC-8432 plug directly into any Series/80 backplane or system and the BLC-416 is a direct replacement for the 16K byte SBC-416.

The BLC-416 and BLC-8432 provide the capability to program MM2716 EPROM's directly. This feature eliminates the need for a separate PROM programmer in OEM systems.

To maintain compatibility with MDS systems not containing a −5V power bus, a low cost regulator may be installed on the board to provide −5V power to the PROM's.

Functional Description

A set of switches and user-selectable BERG™ jumpers on the BLC-416 and BLC-8432 enable 1K or 2K memory block increments and allow base address selection of independent 4K or 8K blocks of memory beginning on any 4K/8K boundary, depending upon the type of memory device installed.

Four easily accessible switches located at the user interface edge of the board allow for timing adjustments when ROM/PROM's overlap RAM. Two other switches are used for disabling 8K or 16K blocks to allow maximum configuration flexibility and memory space allocation.

Full interface and timing logic is provided to allow on-board programming of MM2716 devices. Where a programming voltage of +25VDC is applied through the auxiliary connector, the user can

program any device simply by issuing memory reference instructions from the system CPU. A status indicator and switch on the board display the mode of operation and thus prevent accidental programming.

Specifications

Memory Capacity —	BLC-416	16K bytes in 1K increments
	BLC-8432	32K bytes in 2K increments
Word Size —	8 bits (16-bit jumper selected option)	
Compatible Memory Devices —	MM2308 ROM MM2708 EPROM MM2316E ROM MM2716 EPROM	
Address Selection —	2308/2708 devices — 4K banks on 4K boundaries 2316E/2716 devices — 8K banks on 8K boundaries	
System Bus Interface —	Address, control, and data lines are TRI-STATE™ TTL compatible	
Connectors —		
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers	
Auxiliary	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: AMP P35-14559 TI H311130	

Power —

VDC	Fully loaded 2708 EPROM's	Fully loaded 2716 EPROM's
+5V	0.01 A	1.40 A
−5V	0.72 A	—
+12V	1.04 A	—
−12V	—	—
−25V ± 1V (Programming Voltage)	—	0.12 A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

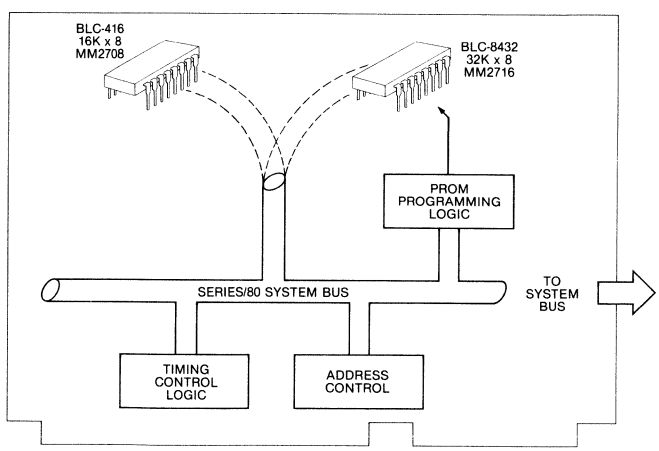
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-416	ROM/PROM Expansion Board factory configured for 2308/2708 devices. Sockets provide a total of 16K bytes of memory.
BLC-8432	ROM/PROM Expansion Board factory configured for 2316E/2716 devices. Sockets provide a total of 32K bytes of memory.

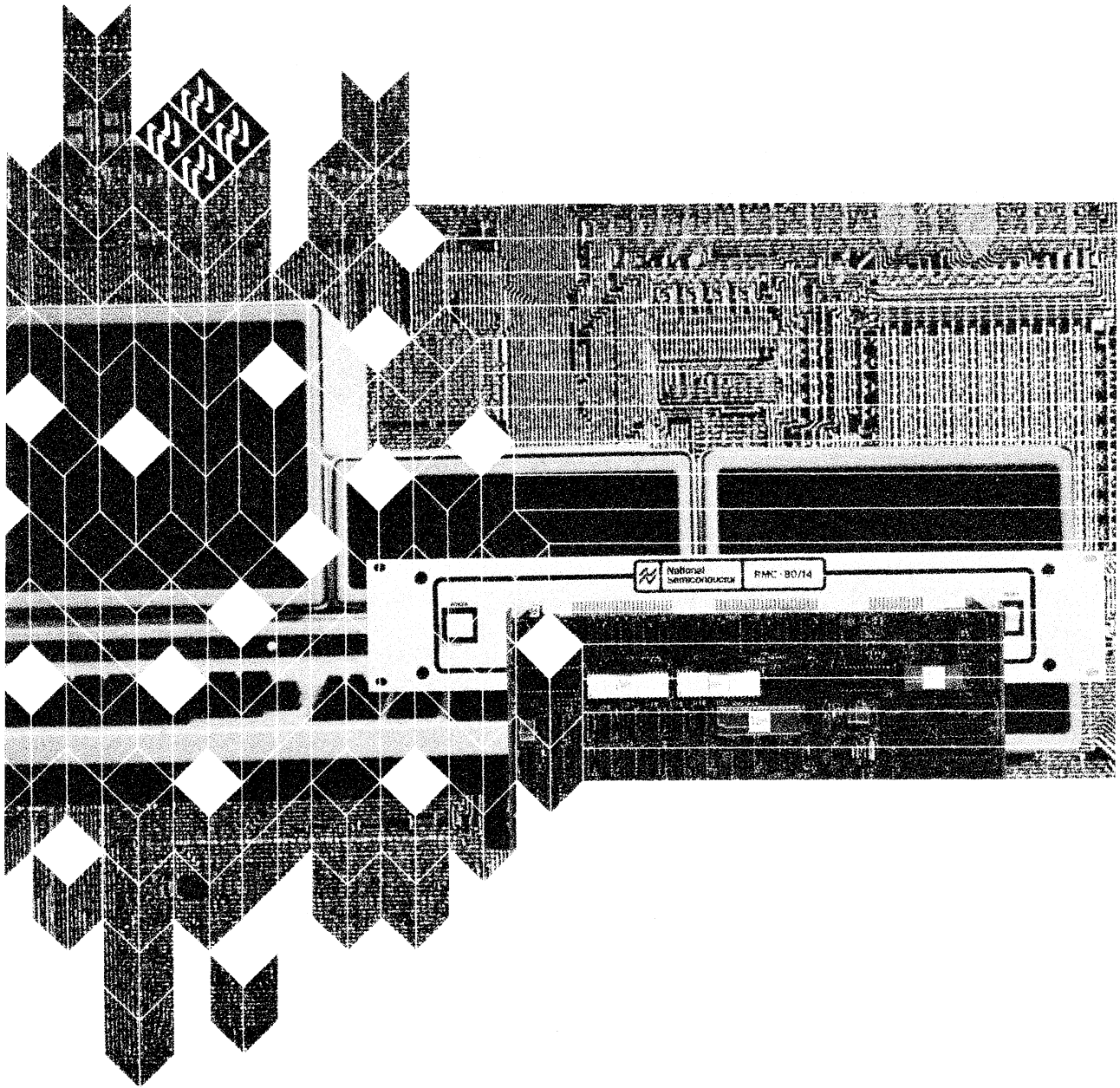
Documentation

420305447-001	BLC-416/8432 16K/32K ROM/PROM Board User's Manual



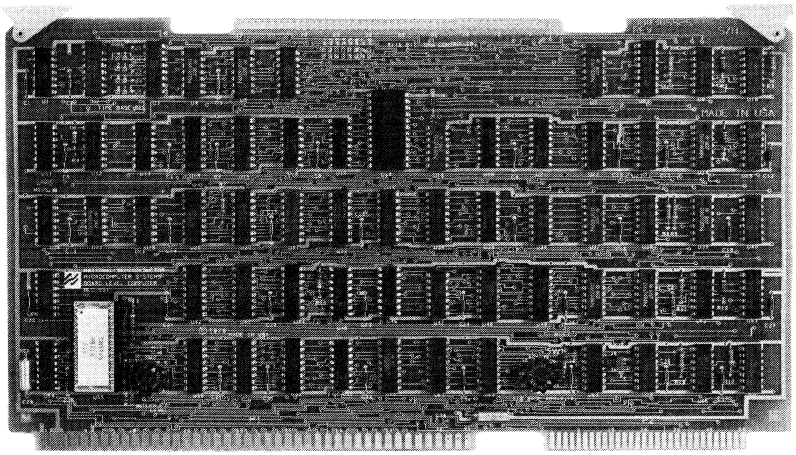
BLC-416 and BLC-8432 Diagram

Section 5
Input/Output
Expansion Boards



National Semiconductor

BLC-501
Direct Memory Access Board



- **Design Flexibility**
  - Interleaved mode data transfer rate up to 330K bytes per second
  - Burst mode data transfer rate up to one million bytes per second
  - Data block transfer length up to 64K bytes
  - Interrupt priority switch selectable to 8 levels
- **Multiprocessor System Capabilities**
  - Bus master capability
  - Software selectable/maskable interrupt operations
  - Memory addressing to 64K locations, software initialized transfers
- **Industry Standard**
  - Bus control logic permits use with all BLC/SBC board level computers
  - Plug-replacement for SBC-501

Product Overview

The BLC-501 Direct Memory Access (DMA) Controller Board complements the broad line of Series/80 products by providing the capability for high speed data transfers between input/output devices and system expansion memory. The DMA board significantly enhances the flexibility of system design with multiple transfer modes and control capability for up to 16 independent devices. The interleaved transfer mode permits data transfers at a maximum rate of 330K bytes per second, while the burst mode permits transfers at a maximum rate of one million bytes per second for high speed applications.

The BLC-501 is fully compatible with BLC/SBC microcomputers and interfaces directly with the system bus for data communication and control. The DMA controller takes full advantage of Series/80 architecture and permits data transfers into the full 64K byte memory range.

Functional Description

The BLC-501 can operate in either the interleaved or the burst data transfer mode.

In the interleaved data transfer mode the DMA controller shares the system bus with the CPU. Each time the DMA controller gains control of the bus, a byte is transferred. In this way the CPU uses the bus on an interleaved basis with the DMA controller. The maximum data transfer rate in this mode is 330K bytes per second.

The burst data transfer mode is employed when maximum data transfer rate is necessary. In this mode, the DMA controller holds the system bus for the entire length of the data block. The maximum data transfer rate in this mode is one million bytes per second. Bus control logic is incorporated to permit use with all Series/80 Board Level Computers. This logic allows the CPU to regain control of the system bus upon completion of data transfer.

The BLC-501 DMA controller is capable of transferring data in 16-bit parallel word size when used with 16-bit word memory modules.

Standard Series/80 instructions control the BLC-501. Output parameters are defined in Table I, input parameters in Table II. Sixteen contiguous addresses are used by the DMA controller. Switch selection is allowed within the range 00_{16} to $F0_{16}$. There are five status and control registers in the BLC-501 DMA board:

- 6-Bit Control Register — Specifies the word size, the busy status, the type of operation to be performed, the data transfer direction, the state of the interrupt system, and the DMA bus usage mode.
- 16-Bit Memory Address Register — Specifies the 16-bit address of the memory location to be accessed. For multiple word transfers, this register is incremented by one after each word has been transferred.
- 16-Bit Length Register — Specifies the unsigned binary value of the total number of words to be transferred (up to 64K). For multiple word transfers, this register is decremented by one after each word has been transferred. Transfers are halted when the length register equals zero.
- 4-Bit Tag Register — A general purpose register that can be used as a command/control register for external devices. With the addition of external decoding logic, up to 16 devices can be interfaced to the BLC-501. To control data transfers, a total of 8 program selected and initiated command strobes are provided — 4 for input and 4 for output. Strobe widths are selected by means of jumpers. Available widths are 100, 200, 400, 800 or 1600 ns.
- 8-Bit Status Register — Provides 4 bits of internal controller status: program interrupt, memory read/write, interrupt status, and controller busy. The remaining 4 bits provide status information from user supplied external devices.

Interrupt requests are passed to the system CPU on one of 9 switch-selected priority levels. These requests may be automatically generated when a data transfer operation is completed (byte for interleaved mode or block for burst mode), when an external device signals an interrupt, or for test purposes. Interrupt enable is program controlled, allowing a high degree of user flexibility.

Table I. Output Parameters

Address	Parameter
Base + 0	Output strobes to external devices
Base + 1	
Base + 2	
Base + 3	
Base + 4	
Base + 5	Not used
Base + 6	
Base + 7	
Base + 8	Set the "SET INT" latch (also sets the INT latch if DMA not busy)
Base + 9	Clears interrupt, DMA busy and SET INT latches
Base + A	Load control register
Base + B	Load tag register
Base + C	Load least significant byte of length register
Base + D	Load most significant byte of length register
Base + E	Load least significant byte of memory address register
Base + F	Load most significant byte of memory address register

Table II. Input Parameters

Address	Parameter
Base + 0	Input strobes to external devices
Base + 1	
Base + 2	
Base + 3	
Base + 4	Read least significant byte
Base + 5	Read most significant byte
Base + 6	Read DMA status word
Base + 7	Input strobe to external devices
Base + 8	Not used
Base + 9	
Base + A	
Base + B	
Base + C	
Base + D	
Base + E	
Base + F	

Specifications

Maximum I/O Data Rates —	One million bytes per second (burst) 330K bytes per second (interleaved)
Maximum Number of Devices —	16
Data Transfer Format —	8-bit parallel or 16-bit parallel
Direct Memory Access Method —	Bus master for burst mode Cycle steal for interleaved mode
Address Range —	64K bytes
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
Device Interface —	TTL compatible, 48 milliamp sink capability using 150 ohm termination

Connectors

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3463-0001
Device	100 contact double-sided edge connector on 0.1 inch centers Recommended mating connectors: Arco AI150WP11 or AE150WP21 Elco 006307100472001 CDC VPB01B50A00A1

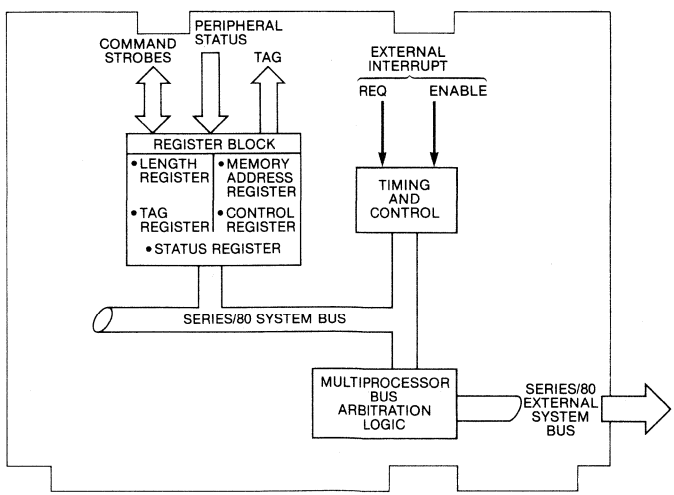
Power —	+5V, 3.35A		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.0 in.	(30.48 cm)
	Depth	0.5 in.	(1.27 cm)
	Weight	14.0 oz.	(396.9 g)

Order Information

BLC-501	Direct Memory Access Board

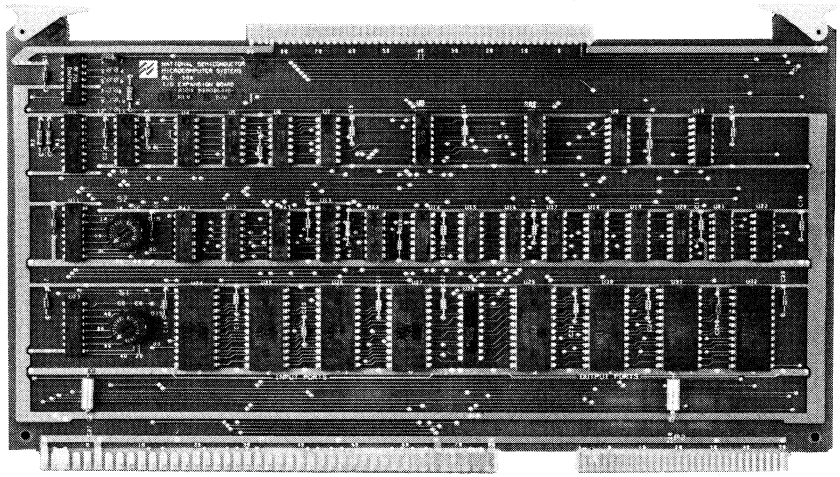
Documentation

420305525-001	BLC-501 Direct Memory Access Board Hardware Reference Manual



BLC-501 Diagram

BLC-508
Input/Output Expansion Board



- **Independently Controlled 8-bit Parallel Ports**
  - Four input ports
  - Four output ports
- **Variable Width Strobed Outputs Permit Synchronization with External Devices**
- **Interrupts for Reduced System Overhead Control**
  - Automatic input port interrupt
  - Eight external available
- **Switch Selected Port Address for System Integration Flexibility**
- **Plug-replacement for SBC-508**

Product Overview

The BLC-508 Input/Output Expansion Board is specifically designed as an economical solution for limited digital input/output application requirements where system computer input/output line capacity is exhausted.

The BLC-508 provides four 8-bit input ports and four 8-bit output ports, each individually addressable. Input and output operation is governed by an on-board strobe with a variable interval to meet a variety of external timing requirements.

The BLC-508 is a plug-replacement for Intel's SBC-508 board.

Functional Description

Input

The input section contains four independent 8-bit ports. Incoming data is latched or unlatched in the input buffer. A buffer full interrupt may be generated to the system CPU to signal data availability.

TRI-STATE™ TTL compatible 8212 devices permit interfacing to a wide range of external devices. Input lines are terminated with 1K ohm pull-up resistors contained in 14-pin DIP modules and mounted in on-board sockets.

Output

The output section contains four independent 8-bit ports. Data is presented to the output port using an I/O write command from the system CPU. Output data is latched in the output buffer. The output strobe to the external device signals the device that data is available.

TRI-STATE™ TTL compatible 8212 devices are used to permit interfacing to a wide range of external devices. Each output line is capable of driving a 48 milliamp load.

The output strobe is variable to permit synchronization with the peripheral device requirements. The strobe pulse width may be jumper selected to 100, 200, 400, 800 or 1600 nanoseconds.

Interrupts

In addition to the interrupt logic associated with the input ports, the BLC-508 contains 8 line external interrupt control. The interrupt driven I/O control feature may be implemented in one of two ways: as a discrete interrupt level or as a single level multi-sourced interrupt. Interrupts are automatically cleared after servicing.

Addressing

Input and output ports use eight contiguous addresses. The base address is the lowest of the eight and is selected by on-board switches. This permits a high degree of system integration flexibility.

Specifications

Number of Input Ports —	4
Number of Output Ports —	4
I/O Port Data Width —	8-bit
I/O Buffer Mode —	Latched
Input Termination —	1K ohm
Output Drive —	48 ma
Output Strobe Width —	Variable 100, 200, 400, 800 or 1600 ns
External Interrupt Capacity —	8
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible.

Connectors

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Input/Output	100 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: Arco AE150WP11 AE150WP21 Eko 006307100472001 CDC VPB01B50A00A1

Power —	+5V, 2.2A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

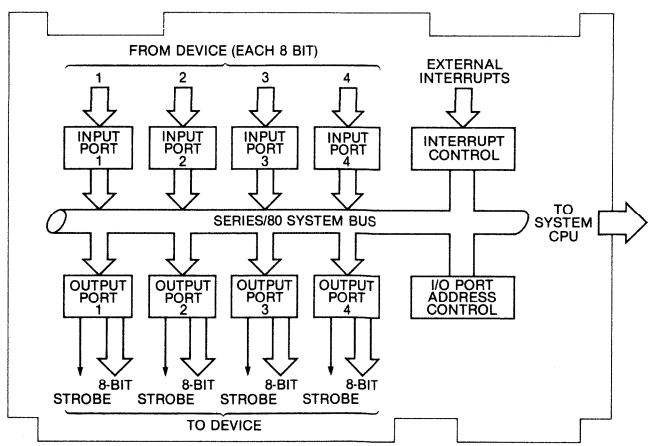
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-508	Input/Output Expansion Board. Contains 8 independent input and output 8-bit parallel ports.

Documentation

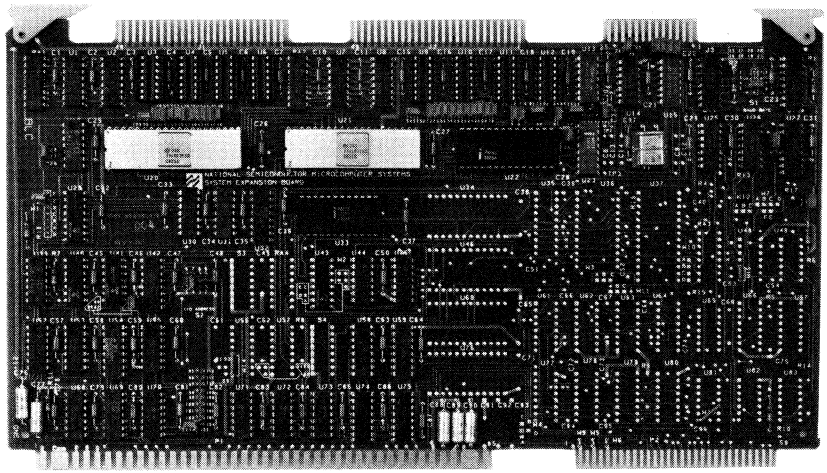
420305448-001	BLC-508 Input/Output Board Hardware Reference Manual



BLC-508 Diagram

National Semiconductor

BLC-517
Input/Output Expansion Board



- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal**
- **Baud Rates of 75 to 38.4K Allow Interfacing to Broad Range of Serial Input/Output Devices**
- **8 Maskable Interrupts for Easy System Control**
- **1 Millisecond Interval Timer for Automatic Time Controlled Sequences**
- **Compatible with BLC/SBC Series/80 Software and Hardware**
- **Plug-replacement for SBC-517**

Product Overview

The BLC-517 Combination Input/Output Expansion Board complements the broad range of BLC/SBC Series/80 Board Level Computers with digital input/output expansion capability.

Both parallel and serial input/output are provided: 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-517 is a plug-replacement for Intel's SBC-517.

Functional Description

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in unidirectional and bidirectional modes. The parallel input/output is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.

- Data read or write to the specified port using strobe or handshake signals created by or transmitted to the interfaced external device.
- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B.

Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line driver and terminator circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

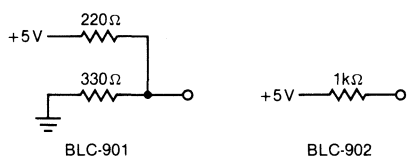


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps. (See Table I.)

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial Input/Output

The serial I/O port control is based on a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4200
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect data parity. Figure 2 illustrates the status word.

7	6	5	4	3	2	1	0
Data Set Ready	Sync Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-517 is designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

Addressing

The BLC-517 uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

Specifications

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Character Length — 5-, 6-, 7- or 8-bit

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous)

75	1200
110	2400
150	4800
300	9600
600	19200

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-001
AMP 2-86792-3

Recommended cables:
BLC-956 Parallel I/O Cable Kit (two 5 foot ribbon cables)

Serial I/O 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power +5V, 2.4A
+12V, 0.04A
−12V, 0.06A

Environmental Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical

Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

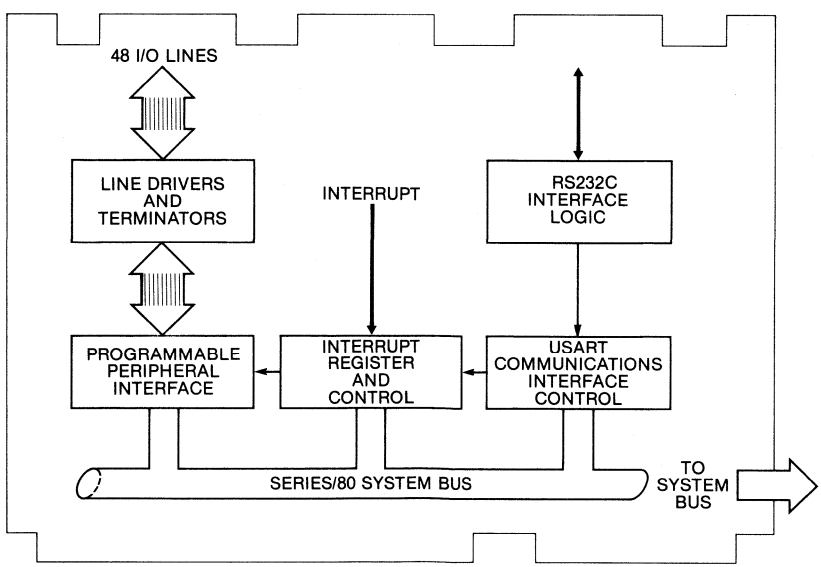
Order Information

BLC-517 Input/Output Expansion Board
Contains 48 parallel and one serial programmable I/O lines, interrupt capability and 1 millisecond interval timer.

BLC-956 Parallel I/O Cable Kit
Contains two 5 foot ribbon cables for connection to parallel input/output board edge connectors.

Documentation

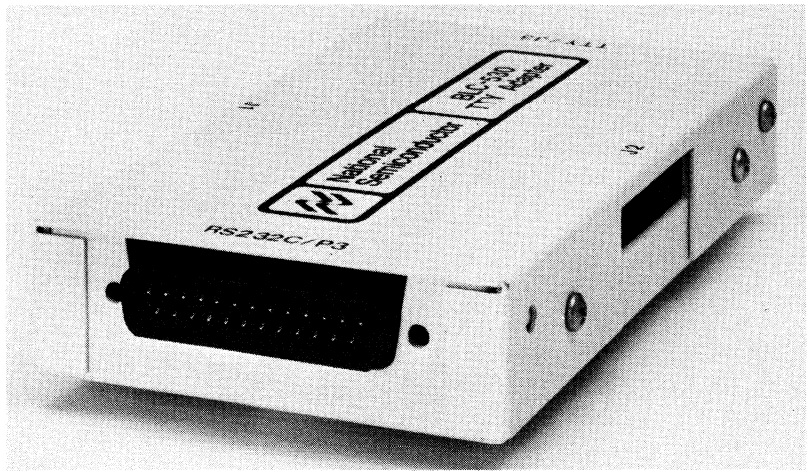
420305376-001 BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual



BLC-517 Diagram

National Semiconductor

BLC-530
Current Loop Adapter



- **Current Loop Conversion for RS232C Serial I/O Channels Extends Series/80 Capability**
- **Data Set or Data Terminal Configuration for Application Flexibility**
- **Fully Compatible with BLC/SBC CPU's and I/O Expansion Boards**
- **Plug-replacement for SBC-530**

Product Overview

National's BLC-530 Current Loop Adapter provides an ideal low cost solution for converting an RS232C serial input-output channel to a 20 milliamperes current loop mode.

Designed in anticipation of the need for application flexibility, the BLC-530 may be used with Series/80 microcomputer and I/O boards when connection is made between the computer and a current loop device, between the computer and a data set, or between a data set and a current loop device.

The BLC-530 easily accommodates a wide variety of applications. It is housed in a small independent container and, thus, does not occupy valuable board slots. This can result in savings in system space and cost.

Fully plug-compatible with Intel's SBC-530, the National BLC-530 may be used with any Intel, National or equivalent Series/80 system.

Functional Description

The BLC-530 Current Loop Adapter is a passive device capable of responding to full or half duplex transmissions without reconfiguration. The line interface on the current loop side of the adapter is optically coupled to assure current loop and RS232C signal isolation.

Current for the current loop is derived from one of two sources. In the standard configuration the adapter derives power from the RS232C serial input-output port 12 volt source. Optionally, the user may reconfigure the adapter to allow power to be supplied from an independent source. A Molex connector is incorporated as an integral part of the adapter for this purpose. Configurations are simply and easily changed by repositioning BERG™ jumpers — no tools or wire are necessary.

The adapter contains two 25-pin connectors for interconnecting the RS232C and current loop channel. Inadvertent cable cross connection is prevented by using a socket-type connector for the RS232C side and a plug connector for the current

loop side. For short distance requirements the BLC-955 I/O Cable Kit is optionally available for use with the BLC-530. The cable kit consists of a 5 foot RS232C interface cable and a 2.5 foot current loop cable. The RS232C cable connector mates to the BLC-530 and to a Series/80 board serial I/O port edge connection. Pin signal assignments are listed in Table I.

Because the BLC-530 is completely self-contained in a separate container it does not require a card cage slot. Instead, the adapter may be located in any desired place and may be stacked.

Table I. BLC-530 Connector Pin Assignments

Pin	RS232C Signal	Current Loop Signal
1	Ground	Ground
2	Transmit Data	—
3	Receive Data	—
4	Request to Send	—
5	Clear to Send	—
6	Data Set Ready	—
7	Ground Carrier Detect	—
11	+12V	—
12	—	TTY Receive
13	Sec Clear to Send	TTY Transmit
14	Sec Transmit Data	—
15	Transmit Clock	—
16	Sec Receive Data	TTY Read Control
17	Receive Clock	—
19	Sec Request to Send	—
20	Data Terminal Ready	—
21	—	TTY Read Control Return
22	Ring Indicator	—
23	−12V	—
24	DTE Transmit Clock	TTY Receive Return
25	—	TTY Transmit Return

Specifications

Transmission Mode — Passive (Half or Full Duplex)

Interface Standard — EIA RS232C

Drive Current — 20 ma loop

Current Source — RS232C I/O Port (optionally from independent source)

Recommended Mating Connector —
RS232C side:
Cannon DB-25S or equal
Current Loop Side:
Cannon DB-25P or equal
Independent Power:
Molex 09-50-7071 with pins or equal

Maximum Current —

	+12V	−12V
RS232C side	30 ma	30 ma
Current Loop side	40 ma	40 ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

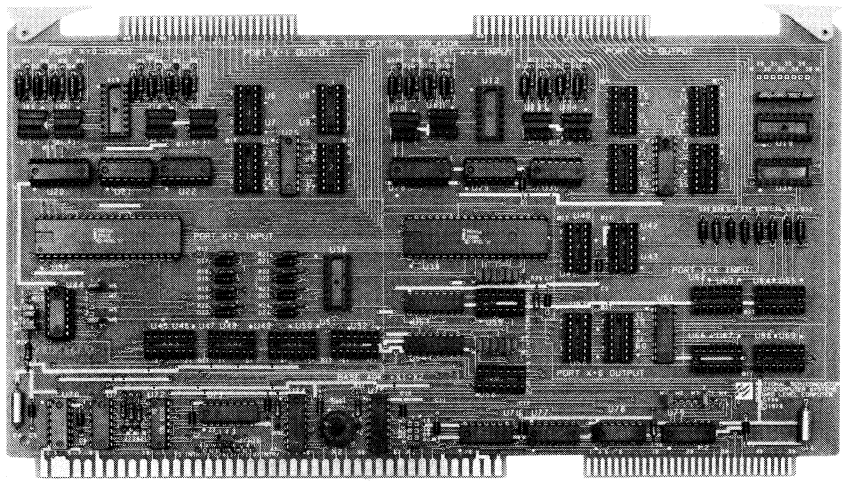
Height	4.85 in.	(12.32 cm)
Width	2.88 in.	(7.31 cm)
Depth	0.92 in.	(2.34 cm)
Weight	9 oz.	(255.2 g)

Order Information

BLC-530 Current Loop Adapter

BLC-955 I/O Cable Kit
Consists of one 5 foot RS232C serial I/O cable and one 2.5 foot current loop cable.

BLC-556
Optically Isolated Input/Output Board



- **Protects Series/80 System from External Voltages of Up to 500 VDC**
- **Eliminates Effects of Ground Loops by Optically Isolating 48 Digital I/O Lines**
- **Sockets for Custom Opto-Isolator Applications**
- **Sockets for I/O Line Drivers and Receivers to Suit User Requirements**
- **Jumper for User Selection of Interrupts**
- **Plug-replacement for SBC-556**

Product Overview

The BLC-556 is an optically isolated, programmable input/output board designed to provide complete isolation between the input/output device and the system computer. Typical applications of the BLC-556 include optical signal connectors to such devices as SCR's, TRIAC's, motors, solenoids and relays.

The board contains 48 program controlled data lines. The 48 data lines are configured into six parallel I/O ports of up to 8 lines per port.

The BLC-556 is a plug-compatible replacement for Intel's SBC-556.

Functional Description

The input/output operations are controlled using two INS8255 programmable peripheral interface modules. Each controls three parallel ports containing 8 lines each. These parallel ports are configured as follows:

- Three 8-line dedicated input ports
- Two 8-line dedicated output ports
- One programmable port configured as:
  - — 8-line input port; or
  - — 8-line output port; or
  - — 4-line input port and 4-line output port

The Series/80 Microcomputer communicates with the BLC-556 using standard input and output instructions. Eight contiguous addresses permit selection of a specific parallel port with the base address switch selectable. Address bits 3 through 7 specify the board base address and bits 0 through 2 identify a specific port on the selected board.

Table I. Input/Output Configuration

Port	1	2	3	Control	4	5	6	Control
Address	Base + 0	Base + 1	Base + 2	Base + 3	Base + 4	Base + 5	Base + 6	Base + 7
Mode	Input	Output	Input	Control Word	Input	Output	Input/ Output	Control Word

In addition to the 48 I/O lines, 8 interrupt lines can be connected to the Series/80 bus interrupt lines. Four external events may be tied to Port 3, Port 6, or both. Before servicing the interrupt, the CPU must read both ports 3 and 6 to identify the interrupting device.

The BLC-556 is designed to accept either differential or single-ended signal sources. The input voltage range is determined by the optical isolator selected and installed. The maximum isolation (limited by board breakdown and tolerances) is:

- Line-to-Line Isolation
  — 230 volts DC or Peak AC
- Input/Output Isolation
  — 500 volts DC or Peak AC

The user has complete freedom within the voltage ranges listed to select and install optical isolators specifically suited to the application. Sockets are provided for easy installation of DIP style circuits. Sockets are also provided for user-installed I/O terminators, input resistor packs and output drivers.

Specifications

I/O Ports — 6

I/O Lines — 48

Input — Single-ended
Differential

Isolation Limit — Line-Line: 230 VDC or Peak AC
I/O: 500 VDC or Peak AC

Recommended Opto-Isolators — Output: 4-pin DIP, LITRONIX ISO-LIT A-30
8-pin DIP, LITRONIX ISO-LIT CT6

System Bus Interface — Address, data and command signals are TRI-STATE™ TTL compatible

System Bus Connector — 86 contact double-sided card cage edge connector on 0.156 inch centers

Input/Output — 50 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
3M 3415-001
AMP 2-86792-3

Power — +5V, 1.6A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

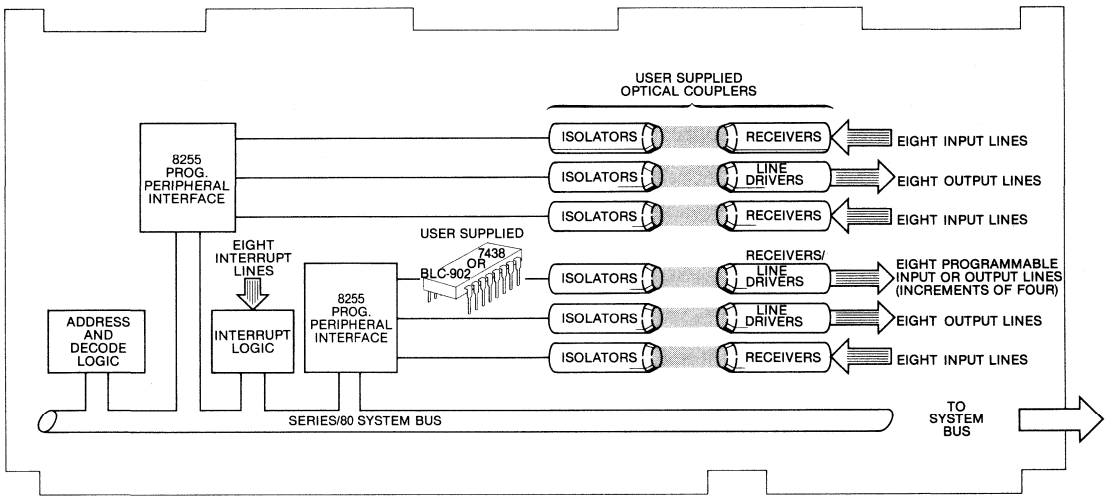
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	12 oz.	(340.2 g)

Order Information

BLC-556 Optically Isolated I/O Board

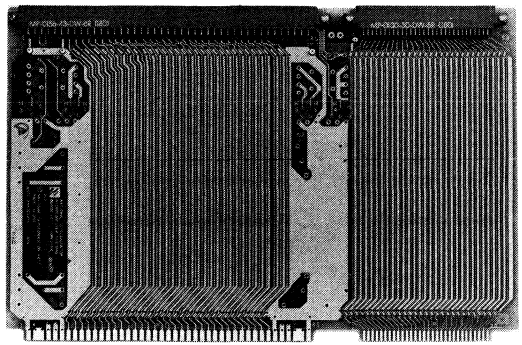
Documentation

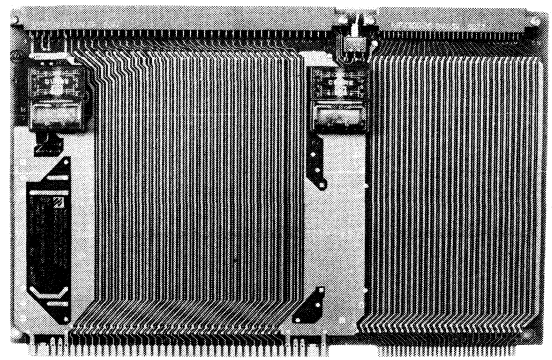
420305559-001 BLC-556 Optically Isolated I/O Board Hardware Reference Manual



BLC-556 Diagram

BLC-610 and BLC-8610 Extender Boards





- **Power Isolation in BLC-8610 Allows Removal/Insertion of Boards without Loss of Data or Functions**
- **Easily Accessible Test Points for Fast Bus and Control Signal Examination**
- **Complete Access to a Series/80 Board for Troubleshooting or Debugging**
- **BLC-610 is Plug-replacement for Intel's MDS-610**

Product Overview

The BLC-610 and BLC-8610 Extender Boards may be used to extend Series/80 family form factor boards beyond the card cage for testing, trouble-shooting or customer debugging.

Each of these boards meets specific user needs: the BLC-610 provides pin-to-pin extension of the BLC-604 or BLC-614 Card Cage backplane and is fully compatible with the Intel SBC-610; the BLC-8610 retains form, fit and function compatibility with the BLC-610 but adds the dimension of power isolation control.

Power isolation enables the user to remove or insert the board under examination without powering down the entire system and losing instruction functions, status, valuable RAM-stored data, etc. Instead, simply flick the power control switch on the BLC-8610 to remove the power bus from the board being examined.

Test points are visible and easily accessible for examination of all backplane signals and power planes.

Functional Description

When installed in a BLC-604 or BLC-614 Card Cage, the BLC-610 provides uninterrupted feedthrough of each pin on backplane connectors J1 and J2 to a Series/80 board inserted in the BLC-610 connector.

The BLC-8610 contains the same features as the BLC-610 except that two relays are employed to allow the user to switch the power lines on and off, as desired, for testing or removal/insertion of Series/80 boards without fear of damage from transients. Power control does not affect the power supplied to the system except for the small amount of current necessary to drive the relays.

Both boards contain ground lugs tied to system ground via the ground bus from J1 and J2. These lugs are provided as a convenience for grounding test instruments.

Board current may be measured on the BLC-610 by removing jumpers and inserting meter probes used on power runs. On the BLC-8610, de-energized relays are "jumpered" and appropriate metering probes are then inserted on selected power runs.

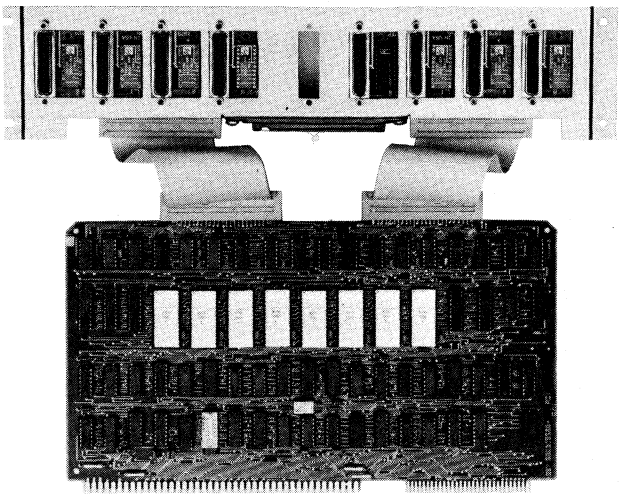
Specifications

		BLC-610	BLC-8610
Current Rating —	+5V	20A	8A
	−5V	5A	2A
	−10V	5A	2A
	+12V	5A	2A
	−12V	5A	2A
Power —	BLC-610: None required BLC-8610: +12V, 60mA		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	8.00 in.	(20.32 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-610	Extender Board
BLC-8610	Extender Board with Power Control

BLC-8534 and BLC-8538 Communications Expansion Boards



- **Full Software Parameter Control for Wide Range of Applications**
  - Asynchronous/Synchronous
  - Data format and parity
  - Baud rates to 19.2K
  - Maskable interrupts
  - Modem Control
- **Four or Eight Independently Controlled Channels for Communications System Flexibility**
- **Error Detection for Each Channel**
- **Meets RS232C Interface Standards**

Product Overview

The BLC-8534 and BLC-8538 Communication Expansion Boards are members of National's Series/80 family and are specifically designed to provide flexible multichannel data communications capability for Series/80 BLC/SBC microcomputer systems.

The BLC-8534 and BLC-8538 provide fully independent programmable asynchronous or synchronous serial communication channels conforming to the EIA RS232C standard, thereby allowing connection to a wide variety of data sets and data terminals. Up to eight independent channels are contained on a single board; each is independently programmable to provide the desired channel characteristics.

Two interrupt lines for each channel are provided for communication channel activity sensing.

Functional Description

Channel control is exercised using standard Series/80 instructions and a Universal Synchronous/Asynchronous Receiver Transmitter (USART) circuit for each channel.

Channels are double buffered for full duplex transmission and contain data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and BERG™ jumpers.

Transmission Characteristics

- Asynchronous
  - — 5-, 6-, 7- or 8-bit characters
  - — Break character generation
  - — 1, 1½, or 2 stop bits
  - — False start bit detect

— Odd, even, or no parity
— Baud rate of 50 to 19.2K
— Ring detect

- Synchronous
  — 5-, 6-, 7- or 8-bit characters
  — Automatic SYNC character insertion
  — SYNC search
  — Baud rate of 50 to 19.2K
  — External synchronization
  — Ring detect

Detection is provided for framing, data overrun and data parity errors.

Either standard programmed I/O or memory mapped I/O program control may be employed. Memory mapped I/O permits memory reference instructions to address the channels. Memory mapped I/O uses a block of 64 bytes of memory; the base address of any 64 byte block is selected using switches on the board. Electronic Industry Association drivers and receivers are used to insure electrical compatibility of channel interfaces.

Interrupts

Two interrupt lines for each channel are available to notify the system CPU when input data is available for transfer (input buffer full), and when data has been transmitted to the serial line (channel output buffer empty). They are individually maskable under program control, allowing a high degree of channel control flexibility. The interrupts may be OR tied or individually sensed, depending on the CPU used or the method of application.

Connectors

An optional connector kit is available to alleviate the need for special user cabling. The kit consists of a connector board which receives up to four RS232C connectors. The board is designed so that each of the four connectors may be user switched from either a terminal or a modem interface. A cable is provided to connect the BLC-8534/8538 to the connector board. The conector boards may be mounted on the back of a rack mounted computer using a special RMC back panel or on a 19 inch rack using the optional RETMA panel.

Specifications

Channels —	4 or 8	
Mode —	Full duplex	
Control —	Independent channel	
Standard Baud Rates —	50	1800
	75	2000
	110	2400
	134.5	3600
	150	4800
	300	7200
	600	9600
	1200	19200
Maximum Baud Rate —	800 KHz	
Baud Rate Clock —	5.068 MHz	
Baud Rate Synchronization —	Internal or external	
Interface Standard —	RS232C	
Interface Signals —	Carrier Detect Clear to Send Data Set Ready Data Terminal Ready Request to Send Receive Clock Transmit Clock Transmit Data Receive Data Ring Indicator	
System Bus Interface —	Data, address and command signals are TRI-STATE™ compatible	
Connectors		
System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers	
Serial Channel —	Two 50 contact double-sided edge connectors on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3	

Power —	Voltage	8534	8538
	+5V	2.0A	2.9A
	+12V	0.13A	0.25A
	−12V	0.12A	0.23A

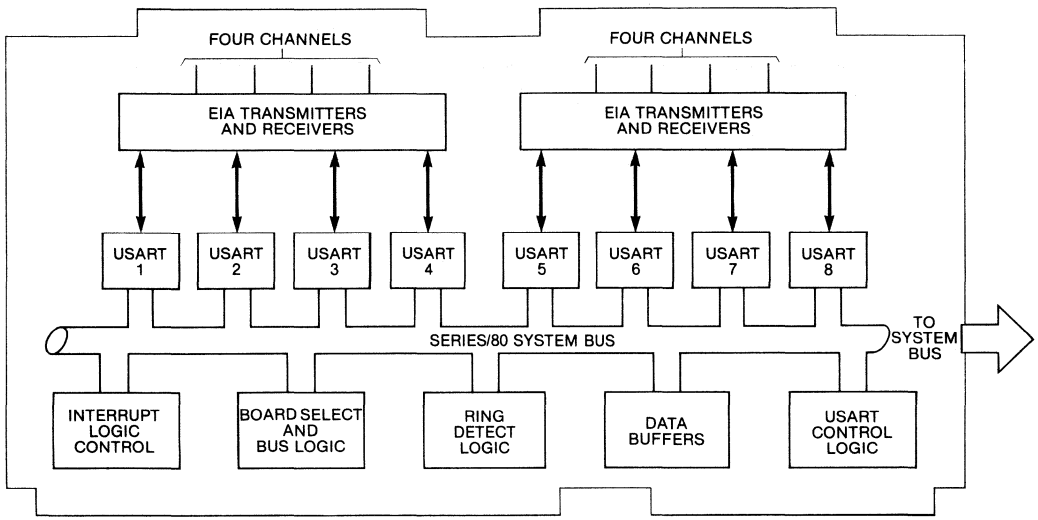
Environmental —	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical —	Height	7.05 in.	(17.91 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 gm)

Order Information

BLC-8538	Eight Channel Communications Expansion Board
BLC-8958	RMC Communications Line Connector Kit (6 in. cable)
BLC-8958-1	RETMA Communications Line Connector Kit (15 ft. cable)
RMC-A001	RMC Communications Back Panel
AEE-001	RETMA Communications Termination Panel

Documentation

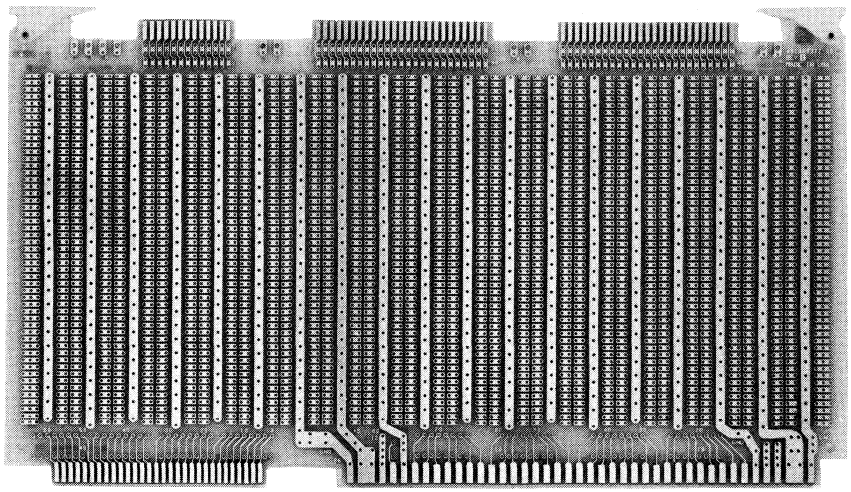
420305528-001	BLC-8534/8538 4 and 8 Channel Communications Expansion Boards Hardware Reference Manual



BLC-8538 DIAGRAM

National Semiconductor

BLC-8905 and BLC-905 Universal Prototyping Boards



BLC-8905

- **Capacity for 108 16-pin DIP's**
- **Choice of Top Edge Connectors**
- **Permits Easier User Construction of Custom Circuitry for BLC/SBC Systems**

Product Overview

The BLC-8905 and BLC-905 provide ready-made, low-cost solutions to the problem of mounting custom circuits in a BLC/SBC computer system. These prototyping boards are designed to accept up to 108 16-pin sockets, integrated circuits, or an equivalent mix of 14, 16, 18, 22, 24, 28, and 40 pin configurations.

Functional Description

The BLC-905 contains one 100 contact top edge connector, and the standard P1 and P2 edge connectors for insertion into a BLC/SBC-604 or -614 card cage backplane.

The BLC-8905 contains two 50 contact connectors and one 26 contact top edge connector.

Specifications

Connectors (BLC-8905)

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Parallel I/O — 50 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3415-0001 or equivalent

Serial I/O — 26 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3462-0001 CRIMP or equivalent

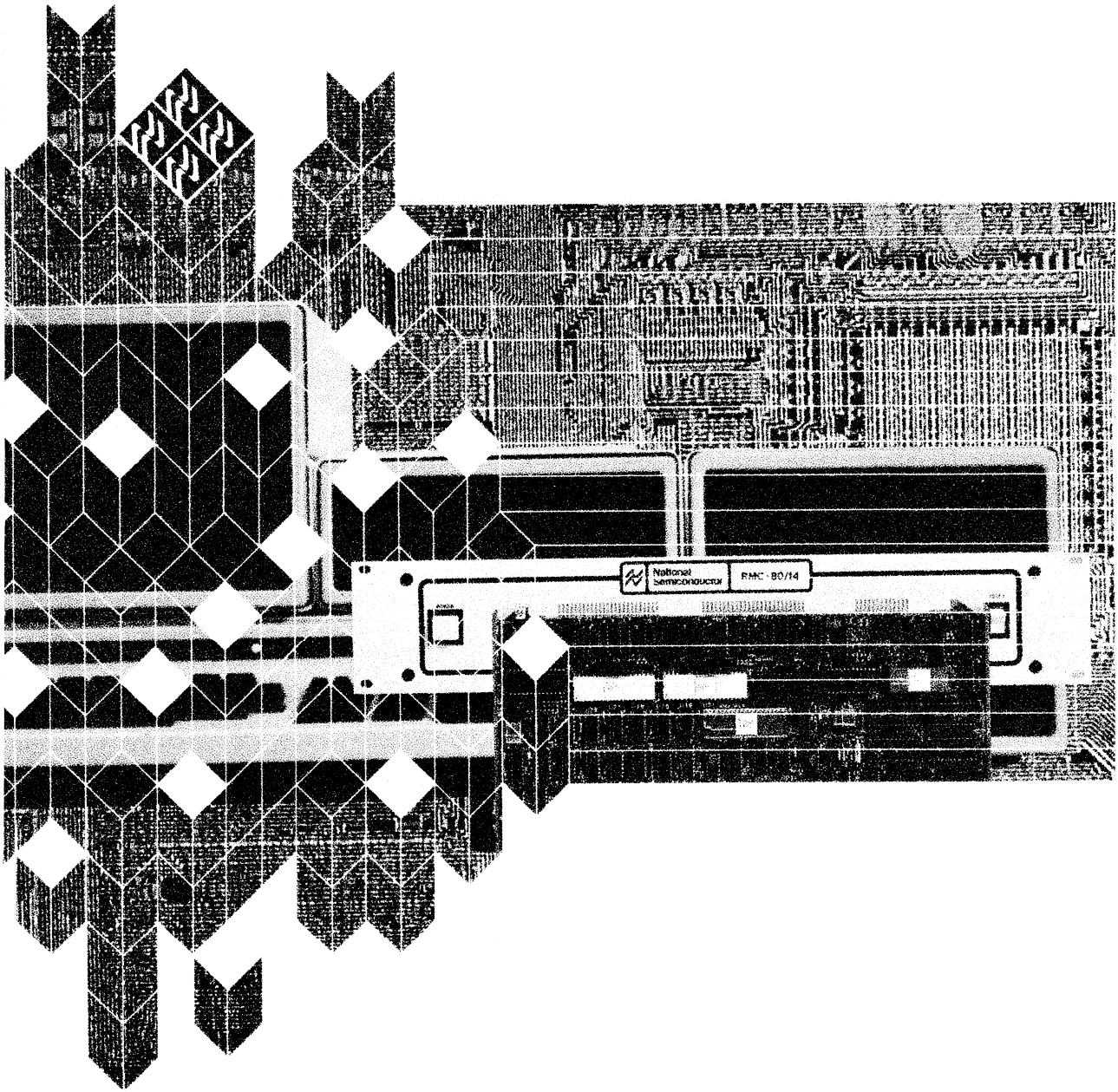
Connectors (BLC-905)

System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers		
Top Edge —	100 contact double-sided edge connector on 0.10 inch centers Recommended mating connector: CDC VPB04B50E00A1E		
Environmental	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	5 oz.	(141.75 g)

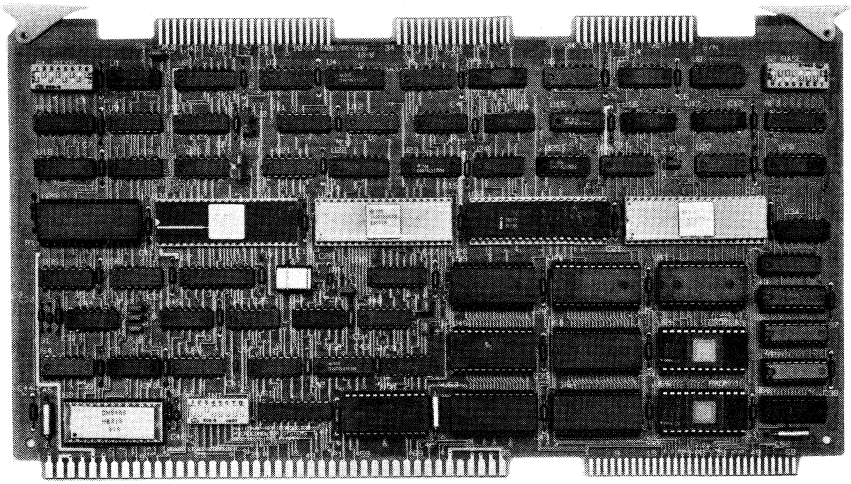
Order Information

BLC-905	Universal Prototyping Board with one 100 contact top edge connector
BLC-8905	Universal Prototyping Board with two 50 contact and one 26 contact top edge connectors

Section 6
Peripheral Controllers



BLC-8201 and BLC-8221 Floppy Disc Controllers



- **Intelligent Non-Volatile Bulk Storage Controller on a Single Series/80 Board**
- **Designed for User Flexibility**
  - DMA data transfers
  - Multi-master bus control
  - On-board 8080A CPU
  - 4K byte EPROM for custom applications, 1K byte RAM
  - Automatic seek error retry
- **Interfaces to Single Density Standard or Mini Floppy Disc Drives**
- **CRC Integrity Error Checking**
- **Large Capacity Systems**
  - Support up to four disc drives
  - Multiple controllers allowed in a single system
- **BLC-8201 — Intel SBC-201 Operating Mode but Requires 70% Less Power**

Product Overview

The BLC-8221 and BLC-8201 Floppy Disc Controllers are members of National's Series/80 family of peripheral device intelligent controllers. The controllers interface directly with a variety of standard and mini size floppy disc drives, adding significant data and program storage capacity to an OEM microcomputer system.

The BLC-8221 and BLC-8201 incorporate the latest in LSI technology to provide a significant amount of on-board control power while minimizing the component count. This results in 70% less power consumption than an SBC-201 controller.

The BLC-8221 is capable of controlling up to four single side recording floppy disc drives. The BLC-8201 can control two recording surfaces. The disc drive heads are automatically unloaded by the controller if there has been no data change in six revolutions. This prevents unnecessary wear of the disc media.

Data integrity is assured by cyclic redundancy checking (CRC) data validation.

Functional Description

The BLC-8221 and BLC-8201 single density floppy disc controllers perform similar operations under direction of the system CPU. The operations include: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC. The system CPU communicates with the controller via programmed I/O and Direct Memory Access (DMA) for commands and data. Once a command is set up and initiated by the CPU, the controller completes the operation without further CPU intervention. The BLC-8201 is designed to communicate with Intel's MDS-DOS system. Standard communications between the system CPU and the controller proceed as follows:

The system CPU prepares a 10 (BLC-8201) or 12 (BLC-8221) byte Input/Output Parameter Block (IOPB) in main memory. The IOPB contains complete instructions to specify the disc operation. (See Figure 1.) The address in main memory for data transfer, read or write disc, interrupt when done, etc., is determined by the IOPB. After building the IOPB in memory, the CPU passes the address of the IOPB using two output instructions. The controller sets its busy status and reads the IOPB from main memory using DMA transfer. When the operation defined in the IOPB is complete, the busy flag is reset and an interrupt is generated, if specified by the IOPB instructions. If the operation specified by the IOPB is a data transfer, data is transferred to and from main memory by DMA. With the BLC-8221 the IOPB may specify buffered data transfers, using the controller's RAM, or unbuffered data transfers. BLC-8201 data transfers are always unbuffered.

Controller logical structure permits the IOPB to define command chaining. In this way, the system CPU can specify any desired sequence of disc operations. The controller completes chained operations autonomously.

Errors are recorded in status bits for condition sensing and recovery. Seek errors are recorded after 3 retries. The IOPB may be used to signify a system interrupt from the controller when an error condition is encountered.

	Content 7	6	5	4	3	2	1	0
Byte 1	Channel Word							
2	Floppy Disc Instruction							
3	Number of Records							
4	Track Address							
5	Sector Address							
6	Main Memory Buffer Address (Low Order Bits)							
7	Main Memory Buffer Address (High Order Bits)							
8	Block Number							
9	Next IOPB Address (Low Order Bits)*							
10	Next IOPB Address (High Order Bits)*							

*Chained operations.

a. BLC-8201 — IOPB Format

	Content 7	6	5	4	3	2	1	0
Byte 1	Disc Number		Interrupt Control		IOPB Length	Disc Command		
2	Number of Sectors							
3	Track Number							
4	Sector Number							
5	Buffer Address Low							
6	Buffer Address High							
7	Sector Length							
8	Data Mark		Retry Level		IBM Format	Buffer Start		
9	Err Flag	Not Used	Block Tag					
10	Not Used		Disc Side	Not Used		Buf or Unbuf	DD or SD	Cmd Chain
11	Next IOPB Address Low							
12	Next IOPB Address High							

b. BLC-8221 — IOPB Format

Figure 1. IOPB Format

Specifications

Data Word Length —	8 bits parallel
Memory Address Range —	64K bytes
Data Transfer Modes —	DMA Programmed I/O
Data Transfer Rate —	Up to 78 KB per second
Data Buffer —	1K bytes
CPU —	INS8080A
Disc Controller —	INS1771
Disc Drive Capability —	BLC-8221: 4 single sided BLC-8201: 2 single sided

Disc Drive Characteristics —

Disc Drive Compatibility	Shugart Model 800 (BLC-8221 and 8201) or 400 Series (BLC-8221) or equivalent
Sector Type	Soft sectored
Recording	Single density
Tracks	77 for 8 inch standard 35 for 5 1/8 inch mini
Sectors per Track for 128 Byte Sector	26 for 8 inch standard 18 for 5 1/8 inch mini
Bytes per Sector	16 to 512 (128 for BLC-8201)
Formatted Storage per Surface	256K bytes for 8 inch standard 80K bytes for 5 1/8 inch mini

System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
Connectors —	
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary	One 60 contact double-sided edge connector on 0.1 inch centers
Mini Size Disc Drives	Two 34 contact double-sided edge connectors on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3463-0001
Standard Size Disc Drives	One 50 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3415-0001
Power —	+5V, 2.0 A −5V, 0.25 A +12V, 0.06 A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

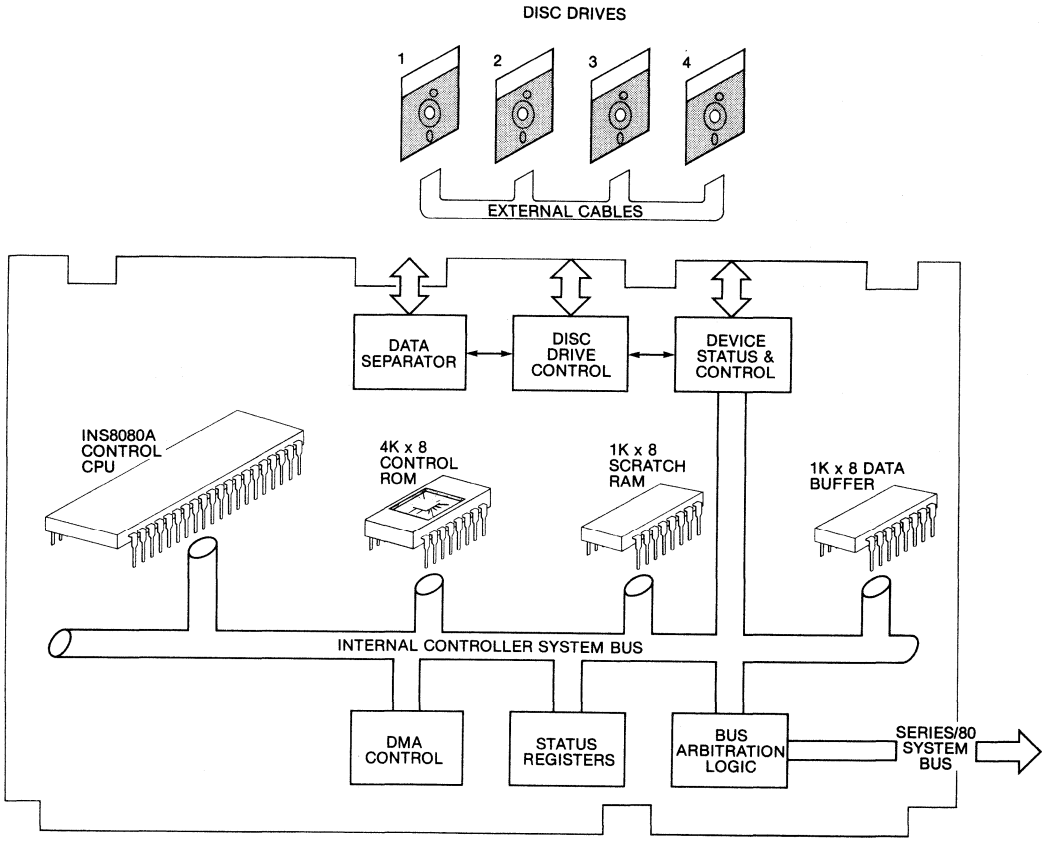
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-8201	Floppy Disc Controller with MDS-DOS Emulation Mode
BLC-8221	Floppy Disc Controller

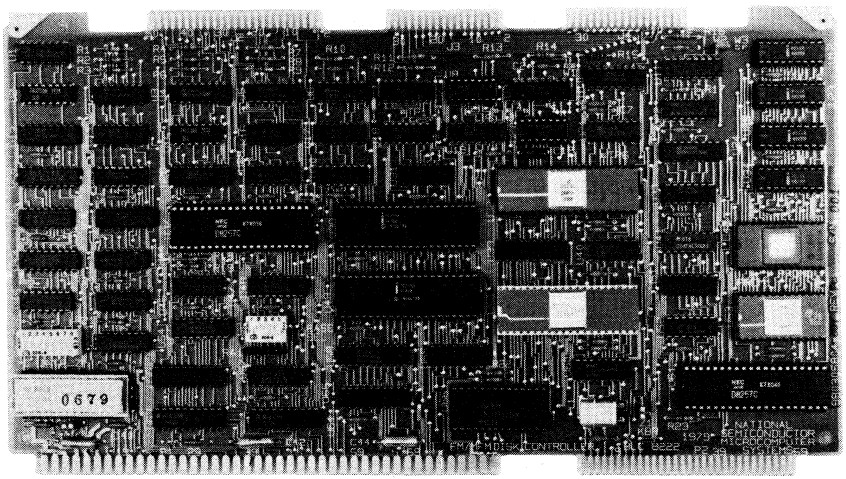
Documentation

420305586-001	BLC-8221/BLC-8201 Floppy Disc Controller Hardware Reference Manual



BLC-8201 and BLC-8221 Diagram

BLC-8222 Double Density Floppy Disc Controller



- **Intelligent Double Density Controller on a Single Series/80 Board**
- **Design Flexibility**
  - Read/Write in IBM System 34 double density (MFM) or IBM 3740 single density (FM) mode
  - FM/MFM selection under program control
  - User definable sector size
  - Switch selectable base addresses allow multiple controller systems
- **Controls Up to Four Dual or Single Sided, Standard or Mini drives**
- **CRC Error Checking with Programmed Re-try**
- **Compatible with Popular Model Shugart Diskette Drives**
- **Bus Transfer Rates Up to 1.3M Bits/Second**

Product Overview

The BLC-8222 Double Density Floppy Disc Controller is a member of National's Series/80 family of intelligent peripheral device controllers. The controller is Multibus™ compatible and provides the Series/80 single board computer user with an easy to use, high performance bulk storage interface. The BLC-8222 uses numerous LSI components, resulting in a powerful single board controller which is economical in terms of space and power consumption, as well as price. Numerous user selectable options are designed in, making the controller highly flexible and easy to use in a wide range of applications requiring large amounts of non-volatile storage.

Functional Description

The BLC-8222 interfaces to the system bus via I/O, DMA, and interrupts. The I/O interface is used to pass information from the system CPU to the controller as well as to allow the CPU to read controller status. The DMA interface is used to transfer control blocks into on-board memory and to transfer data blocks between on-board memory and system memory. The disc controller interrupts are used to inform the system of the completion of operations and changes in disc status.

All diskette operations are initiated by the system processor by standard I/O commands. Once initiated, the disc operations are completed by the

controller with no further interactions. The processor performs the following steps to initiate the complete disc operations:

1. Prepares and stores in system memory an I/O Parameter Block (IOPB) for each operation to be performed. The IOPB contains complete instructions specifying the disc operation. If multiple operations are to be performed, IOPBs can be linked together.
2. Passes the memory address of the IOPB to the controller through two I/O ports.
3. Processes the resultant information from the controller upon completion of the disc operations. The system processor can test for the completion of the disc operation by polling the BUSY status bit through the controller I/O interface or by enabling the controller interrupt through the IOPB and servicing the interrupt generated by the controller.

Operations performed by the disc controller include: read, write, sequential or random format, controller to memory read/write, and test. Controller logical structure permits the IOPB to define command chaining. The system CPU can specify any desired sequence of disc operations and the controller then completes the chained operations autonomously.

Programming

The BLC-8222 appears to the system bus as a set of eight consecutive I/O devices. The I/O addresses range from BASE + 0 to BASE + 7, where BASE is a switch selectable decoding of the upper five I/O address bits. This I/O interface is used by the system processor to send COMMAND bytes to the controller and to read controller STATUS bytes. The relative address decoding and bit assignments for the I/O interface are shown below.

STATUS BYTES

	7	6	5	4	3	2	1	0
BASE + 0	ERROR GROUP				ERROR CODE			
BASE + 1	BUSY	ERROR	RETRY	X	Drive 3 Ready	Drive 2 Ready	Drive 1 Ready	Drive 0 Ready
BASE + 2	X	X	Block tag of last command executed with an error					

INTERFACE COMMANDS

	7	6	5	4	3	2	1	0
BASE + 1	IOPB Memory Address Low							
BASE + 2	IOPB Memory Address High							
BASE + 7	X	X	X	X	X	X	X	X

The start of any diskette operation occurs when the system processor writes to the controller, through I/O addresses BASE + 1 and BASE + 2, the starting address of the IOPB. The IOPB can be located anywhere in main memory and consists of either six or twelve consecutive bytes of control information. The relative positioning of the bytes within the IOPB are as shown below:

IOPB

	7	6	5	4	3	2	1	0
BYTE 1	Disc Number		Interrupt Control		Length	Disk Command		
2	Number of Sectors							
3	Track Number							
4	Sector Number							
5	Buffer Address Low							
6	Buffer Address High							
7	Sector Length							
8	Data Mark		Retry Level		IBM Format	Buffer Start		
9	BTR	X	Block Tag					
10	X	X	Disc Side	X	X	X	DD or SD	CMD Chain
11	Next IOPB Address Low							
12	Next IOPB Address High							

Specifications

Data Word Length —	8 bits parallel
Memory Address Range —	64K bytes
Data Transfer Modes —	DMA, programmed I/O
Data Transfer Rate —	Up to 1.3M bits/second
Data Buffer —	2K bytes
CPU —	INS8080A
Disc Controller —	INS1791
Disc Drive Capability —	4 single or dual sided
Disc Drive Characteristics	
Compatability —	Shugart Models 400, 400L, 800 and 850
Sector Type —	Soft sectored
Recording —	Single or double density
Tracks —	77 for 8 inch standard
Bytes per Sector —	128, 256, or 512 bytes software selectable
Formatted Storage Capacity —	Shugart 400 — 80K bytes 400L — 80K/160K bytes 800 — 256K/512K bytes 850 — 512K/1M bytes
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible

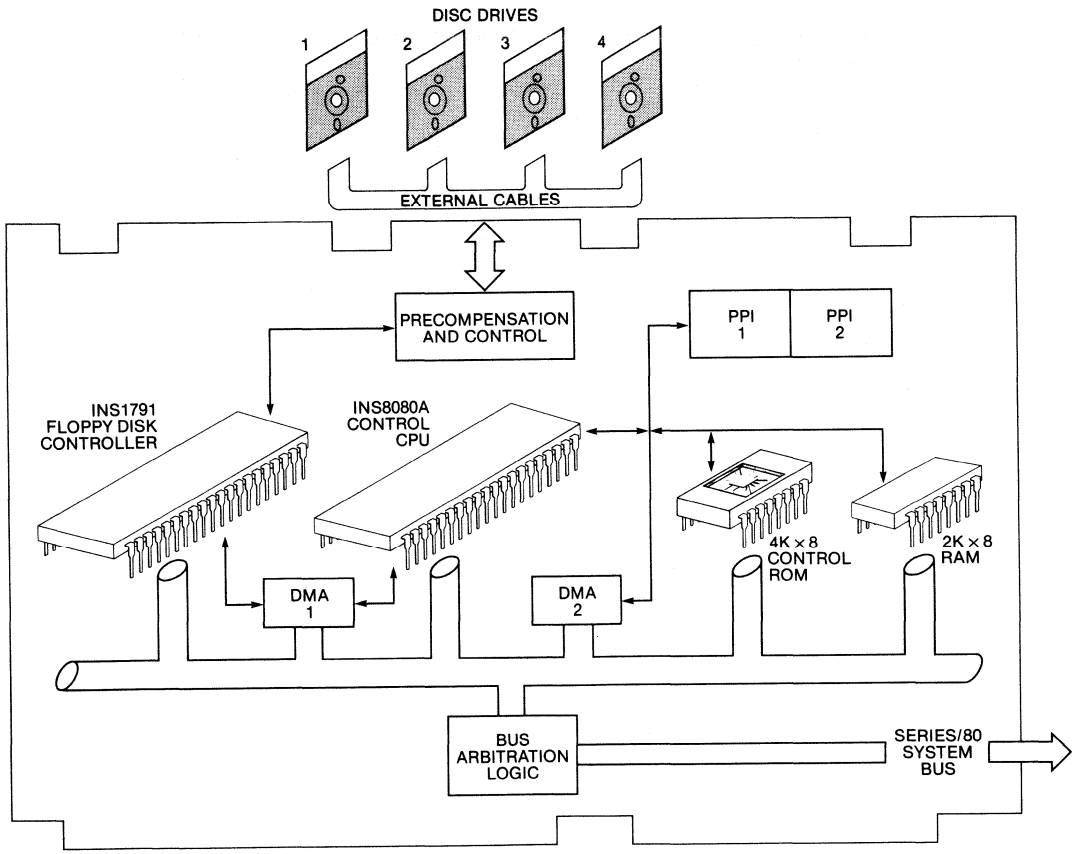
Connectors —	
System Bus	86 contact double sided edge connector on 0.156 inch centers
Auxiliary —	One 60 contact double-sided edge connector on 0.1 inch centers
	Recommended mating connector: 3M "Scotchflex" 3415-0001
Power Requirements —	+5VDC ± 5% 1.75 A +12VDC ± 5% 75 ma −5VDC ± 5% 1 ma
Environmental Characteristics —	Temperature 0 °C to 55 °C Humidity 0-90% non-condensing

Order Information

BLC-8222	Double Density Floppy Disc Controller

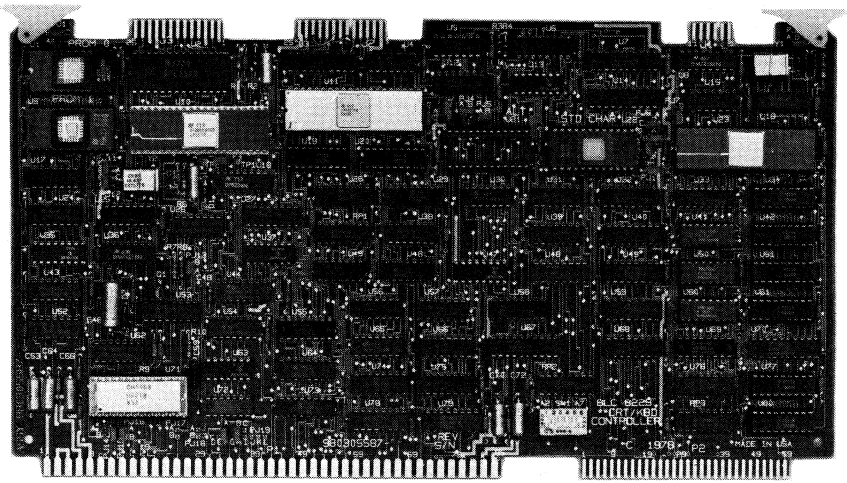
Documentation

420305804-001	BLC-8222 Floppy Disc Controller Hardware Reference Manual



BLC-8222 DIAGRAM

BLC-8228 and BLC-8229 Video Monitor/Keyboard Controllers



- **Intelligent Controller on a Single Series/80 Board**
- **Designed for User Flexibility**
  - DMA transfers for rapid screen update
  - Interrupt control
  - On-board 8080A CPU and control ROM
  - 1K byte scratch pad RAM
  - Complete editing function, control logic and scrolling
  - EPROM sockets for user-defined alternate character set
  - Programmable display attributes: blink, blank, inverse video and alternate character set
  - Full software cursor control
  - 3 wire video output
- **On-Board Video Refresh Memory**
- **Full 128 ASCII Character Set**
- **24 Line (BLC-8228) or 25 Line (BLC-8229) by 80 Character Display Array**
- **Selection of Display Matrix**
  - 5 by 7 — BLC-8228
  - 7 by 9 — BLC-8229
- **Compatible with All Series/80 Boards and Card Cages**

Product Overview

The Video Monitor/Keyboard Controller is a member of National's Series/80 family of peripheral device intelligent controllers. It is fully compatible with all National Series/80 boards and plugs directly into any Series/80 card cage backplane or system. The controller is available in two models, BLC-8228 and BLC-8229. The BLC-8228 provides a 5x7 dot matrix character while the BLC-8229 provides a 7x9 dot matrix character.

All that is required to make the BLC-8228 or BLC-8229 an intelligent CRT terminal is the addition of a standard ASCII encoded keyboard and a low cost monitor. The BLC-8228 provides a display array of 24 lines by 80 characters, while the BLC-8229 provides a 25-by-80 array. The character generator consists of a 128 upper and lower case ASCII character set. The controller can also accommodate a user-supplied custom alternate character set which may be software selected on a character-by-character basis.

Full software cursor control (up, down, left, right, home, set, indirect, sense) and screen formatting codes are included to yield a very powerful screen editor. Although on-board firmware provides numerous special editor functions, the user may implement custom editing and formatting functions by writing his own firmware. (See Table I for standard functions.)

Each character is assigned one of four attributes: blink, blank, inverse or alternate character. Scrolling is software selectable for each display line. In this way selected lines can be excluded from scrolling. Non-displayable ASCII control codes (e.g., ACK, EOT, etc.) may be displayed on the monitor and occupy only one display character position. An on-board tone generator is available for connection to an external speaker. The cursor may be represented as block inverse or underscore (blinking or non-blinking).

Functional Description

The BLC-8228 and BLC-8229 contain an on-board 8080A CPU with up to 4 KB of space for instruction ROM/PROM (2K bytes using MM2708 PROM or 4K bytes using MM2716 EPROM), a 1K byte scratch pad RAM, 2K character buffer and 2K x 4 bits buffer RAM for character attribute codes, 2K byte refresh RAM, a CRT controller chip, and 2 sockets for a standard and an alternate character generator.

Characters generated by the user's encoded keyboard enter the controller as an 8-bit parallel transfer under interrupt control. The controller transmits the character to the host CPU, which then processes it and transmits it back for display.

Communication between the host CPU and the controller is accomplished in byte parallel via the main system data bus. An 8-bit status register is also available to the host CPU via the main system data bus. Character data can be moved between the controller's RAM buffer and main system memory in DMA mode to provide high speed data transmission.

One of two character generator PROM's (standard or alternate) is enabled according to the state of the controller font bit.

The controller provides 3 host maskable interrupts, CRT Ready, Keyboard Ready and ERROR, to the host CPU. Each of these may be jumpered to any of 9 main bus interrupt lines. The interrupt information is also available to the system by reading the status register contents.

Video output consists of separate horizontal sync, vertical sync and video out signals. STEP-SCAN™ is a jumper selectable option which produces a screen display with more than one line of space between rows and no inter-leaving blank lines between rows and columns. STEP-SCAN is typically used in normal character applications where the extra space produces an exceptionally clear and easy-to-read display.

Controller integrity is assured by execution of on-board tests which are automatically activated upon receipt of a system reset. The validation testing exercises the controller RAM, PROM and I/O display ports.

Table I. Editor Functions and Software Switches (On/Off)

CURSOR	Set Cursor Set Cursor Indirect Set Cursor On Set Cursor Off Sense Cursor Move Cursor Right Move Cursor Left Move Cursor Up Move Cursor Down Move Cursor Home
LINE	Enter Insert Line Insert Line Exit Insert Line Delete Line Erase to End of Line Auto Carriage Return On/Off (80 column)
CHARACTER	Enter Insert Character Insert Character Exit Insert Character Delete Character Destructive Backspace On/Off Upper Case On/Off
TAB	Set Tab Clear Tab Clear All Tabs Back Tab Destructive Tab On/Off Destructive Back Tab On/Off
DMA	Enter DMA Mode Enter DMA With Count Exit DMA Mode Privileged Mode On/Off
SCROLL	Roll Up Roll Down Home & Clear Erase to End of Screen Fix Line Unfix Line Unfix All Lines
ATTRIBUTES	Set Attributes Write Attributes Load Attribute Memory Dump Attribute Memory
SCREEN	Dump Screen Memory Load Screen Memory
MISCELLANEOUS	Write Character Reset Call Subroutine Set LED Set/Reset Software Switches Clear Keyboard FIFO Buffer

7	6	5	4	3	2	1	0
Keybd Ready	CRT Ready	Error Flag					
			Error Code				

a. Status Register

7	6	5	4	3	2	1	0
Keybd Ready Intrpt Enable	CRT Ready Intrpt Enable	No Error Intrpt Enable	Not Used	Not Used	Not Used	Not Used	Not Used

b. Interrupt Mask Register

7	6	5	4	3	2	1	0
Char/ Control Code							
				Data			

c. Data Word

Figure 1. Status, Interrupt and Data Format

Specifications

Data Transfer Mode — DMA or Programmed I/O

DMA Transfer Rate — Up to 78K bytes per second

CPU — INS8080A

Video Monitor Controller — DP8350 (5x7)
DP8353 (7x9)

Scratch Pad Buffer — 1Kx8-bit RAM

Attribute Buffer — 2Kx4-bit RAM

Instruction ROM — 2Kx8-bit (standard firmware MM2708)
4Kx8-bit sockets (MM2716 as a user-implemented option)

Character Generator — Standard 128 character upper/lower case ASCII
May also contain user-implemented character set (INS2708 or 2716)

Keyboard Input Port — 8 data lines and 1 strobe from keyboard

Audio Signal Generator — 2500 Hz for 0.15 seconds (BLC-8228)
3300 Hz for 0.15 seconds (BLC-8229)

Special Function Register — 4 bits wide for external LED indicators or custom flags

Display — 24 rows by 80 columns with 5x7 dot matrix (BLC-8228)
25 rows by 80 columns with 7x9 dot matrix (BLC-8229)
Individual character attributes:
- blink (2 Hz)
- blank
- inverse video
- alternate character set

Cursor types (jumper selectable):
- block
- blinking
- non-blinking
- underscore (BLC-8229 only)
- none

Frequency 50 or 60 Hz

Address — Switch select four of 256 available I/O addresses

Bus Interface —

System — Address, data and command signals are TRI-STATE™ TTL compatible

Video Monitor Interface — Horizontal and vertical sync are TTL compatible
Video Out:
- Low — 0.2V
- Med — 1.6V (inverse character background)
- High — 2.2V

Frequency:
- 15.9 KHz (BLC-8228)
- 19.2 KHz (BLC-8229)

Connectors —

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers
Recommended mating connector:
- CDC VPB01E43A00A1 or equivalent

Keyboard — 26 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
- 3M 3462-0001, TI H3/2113 or equivalent

Video Monitor — 12 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
- AMP 2-583717-1 or equivalent

Power — +5V, 4.90A
−5V, 0.91A
+12V, 0.22A
−12V, 0.30A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

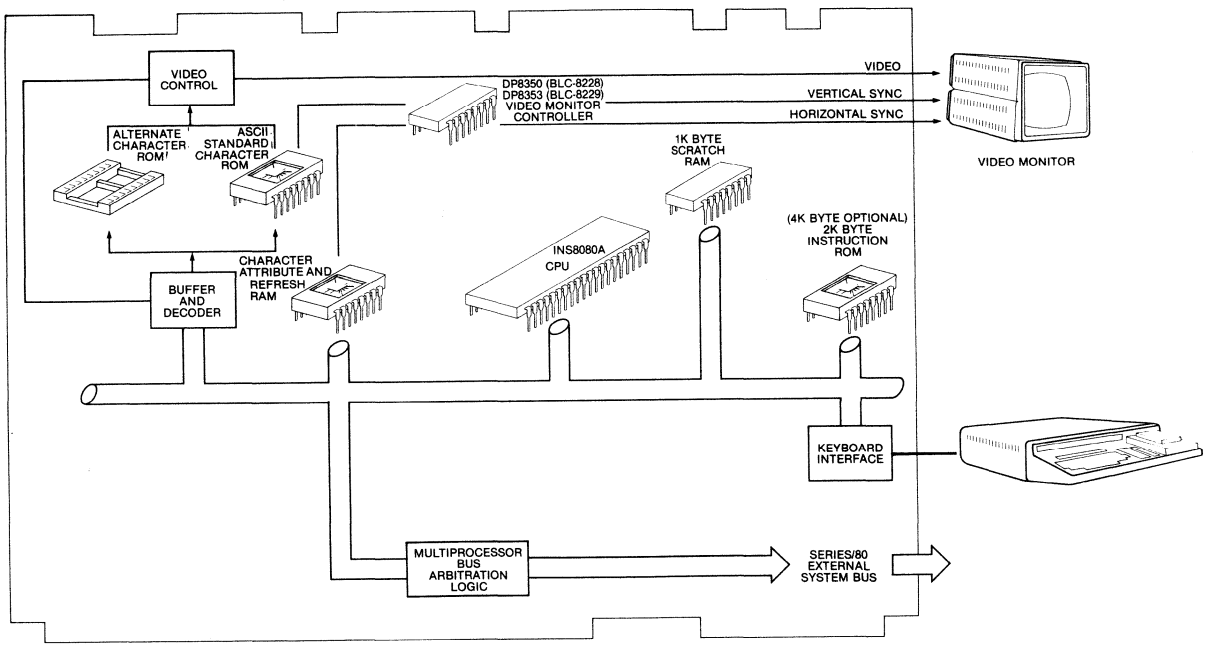
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-8228	Video Monitor/Keyboard Controller with 5x7 dot matrix character generator
BLC-8229	Video Monitor/Keyboard Controller with 7x9 dot matrix character generator

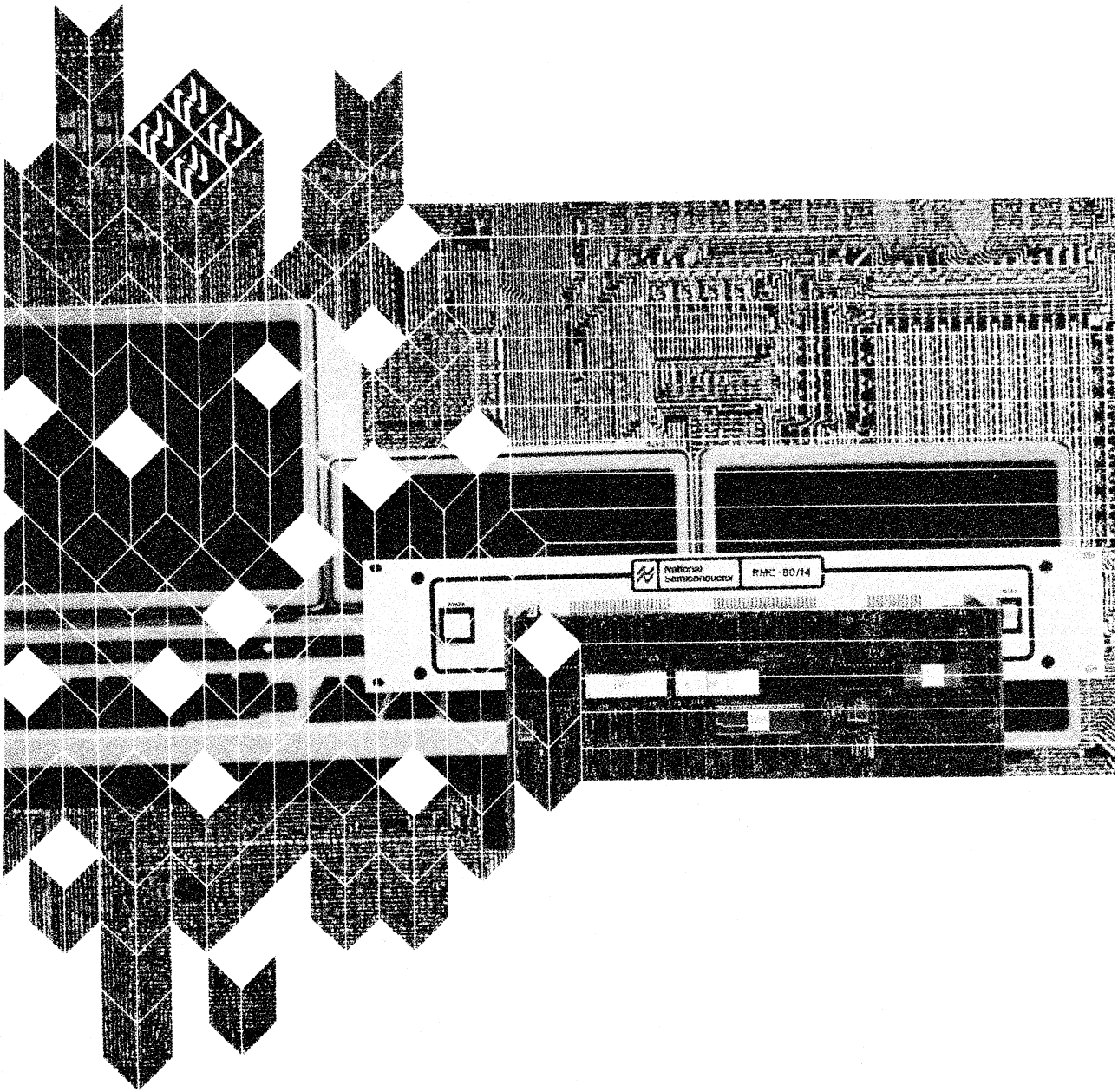
Documentation

420305587-001	CRT/Keyboard Controller Board Hardware Reference Manual

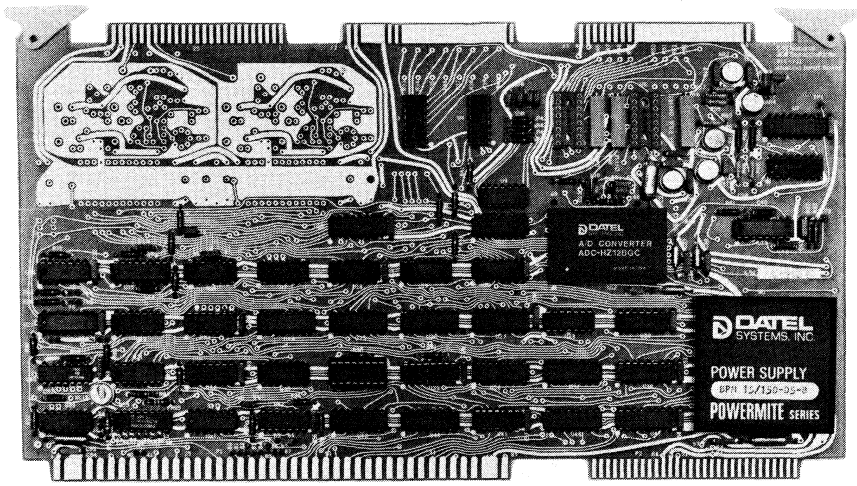


BLC-8228 and BLC-8229 Diagram

Section 7
Analog Input/Output Boards



BLC-711
Analog Input Board



- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - Voltage or current mode inputs
  - Sequential, random and single channel scan modes
- **50 KHz Sample Rate Permits Use in Wide Range of Applications**
- **12-bit Resolution with 0.05% Overall Accuracy for Precise Measurements**
- **On-board Pacer Clock or External Synchronization of Sampling for System Flexibility**
- **Programmable Gain Amplifier Accommodates Wide Range of Systems**
- **Plug-replacement for SBC-711**

Product Overview

The BLC-711 Analog Input Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process control applications.

The BLC-711 provides multiple analog input capability. Analog input functions allow data sampling at a rate of 50,000 samples per second and storage of equivalent digital values for subsequent processing. The BLC-711 is equipped with sample and hold circuitry, and accuracy of conversion is assured by holding the input sample constant until conversion is completed. Analog inputs may be sampled in a random, sequential, or single channel repetitive mode.

The board contains a high resolution 12-bit analog converter, 16 single-ended or 8 differential input channels, programmable gain amplifier, and the sample and hold function. The analog input capacity is expandable to 32 single-ended or 16 differential channels.

The BLC-711 is a plug-compatible replacement for Intel's SBC-711.

Functional Description

Standard Series/80 instructions control analog input channels. Memory mapped I/O simplifies the transfer of data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O, a segment of 16 contiguous addresses is predefined by the user and set on the board via jumpers. These addresses may be on any even 16 byte boundary within the 64K bytes of available address space. If these addresses overlay system memory addresses, memory inhibit logic prevents address contention for memory mapped I/O addresses.

Analog Input

Analog to digital (A/D) conversion is initiated by a Write command to the Multiplexer Address Register (MAR). The bit pattern of the MAR specifies the gain and the specific channel to be converted. The Command Register (CR) is then loaded with a bit pattern that enables conversion and the desired interrupts. Bits in the Command Register also specify pacer clock/external trigger, the board busy bit, and enabling sequential scan.

If the sequential scan feature is enabled, input channels will be sequentially converted until the channel address in the Last Channel Register (LCR) is reached.

Data sent to the Command Register can be read back by issuing a Read command to the Status Register (SR). In addition to verifying the last command word sent to the Command Register, the status also signifies that conversion has been completed or that the last channel has been reached.

After analog conversion is complete, the corresponding digital data value is read from the converter register. The first byte contains the low order 4 bits (bits 0 to 3) of the digital representation; the second byte contains the 8 high order bits (bits 4 to 11).

The selected analog input is applied to the A/D converter through a software controlled programmable gain amplifier which provides gains of X1, X2, X4, or X8, and a sample and hold amplifier. With the A/D converter jumper selected for +5V, +10V, ±5V, or ±10V full scale input voltages, the gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable Gain Full Scale Values

Gain Selected	Voltage Range Selection			
	+5V	+10V	±5V	±10V
X1	+5V	+10V	±5V	±10V
X2	+2.5V	+5V	±2.5V	±5V
X4	+1.25V	+2.5V	±1.25V	±2.5V
X8	+0.625V	+1.25V	±0.625V	±1.25V

Sampling is controlled in one of three ways: by program instruction (writing the multiplexer address to an analog input channel), by an internal sample timer (pacer clock), or by external event synchronization (external trigger). The pacer clock may be jumper configured to provide timing intervals from 975 microseconds to 1 second.

Interrupts to the system CPU may be generated upon completion of either a channel sample conversion or a sequential channel scan. This relieves the system CPU of continuous status scanning.

The analog input control parameters are illustrated in Figure 1.

7	6	5	4	3	2	1	0
Gain Select	Gain Select	Not Used	2^4	2^3	2^2	2^1	2^0

Channel Select

Gain	Bit 7	Bit 6
X1	0	0
X2	0	1
X4	1	0
X8	1	1

a. Multiplexer Address and Gain Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Not Used	2^4	2^3	2^2	2^1	2^0

Last Channel Address

b. Last Channel Sampled Address Format

7	6	5	4	3	2	1	0
Not Used	Not Used	End of Conv. Intrpt	End of Scan Intrpt	Clear Busy	Exit Trig Enable	Auto Incr Enable	Start/ Stop

c. Command Register Byte Format

7	6	5	4	3	2	1	0
Conv. Done	Scan Done	End of Conv. Intrpt	End of Scan Intrpt	Busy	Exit Trig Enabl	Auto Incr Enabl	Start/ Stop

d. Status Register Byte Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Clear End of Conv. Intrpt	Clear End of Scan Intrpt	Clear Pacer Clock	Not Used	Not Used	Not Used

e. Clear Interrupts Format

Address	Write Command Description
Base + 0	Load Command Register (CR)
Base + 1	Load Multiplexer Address Register (MAR)
Base + 2	Load Last Channel Register (LCR)
Base + 3	Clear Interrupts

Address	Read Command Description
Base + 0	Read Status Register (SR)
Base + 1	Read Multiplexer Address Register (MAR)
Base + 4	Read LS Byte, A/D (ADCR)
Base + 5	Read MS Byte, A/D (ADCR)

f. Memory Mapped Addressing

Figure 1. Analog Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5 VDC power input to the ±15 VDC required by analog circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-711 to allow testing the analog circuits.

Specifications

Scan Mode —	Sequential; Random; Single Channel Repeat
Channels —	16 single-ended or 8 differential
Channel Resolution —	11 bits plus sign, 2-s complement bipolar 12 bits, unipolar or offset binary
Full Scale Range Volts —	0 to +0.625; +1.25; +2.5; +5 0 to +1.25; +2.5; +5; +10 ±0.625; ±1.25; ±2.5; ±5 ±1.25; ±2.5; ±5; ±10
Programmable Gain —	X1, X2, X4, X8
Sample and Hold —	
Aperture Time	Less than 100 nanoseconds
Uncertainty Time	20 nanoseconds
Acquisition	8 microseconds
Throughput Rate —	24 KHz
A/D Conversion Speed —	50 KHz
Overall Accuracy — (25 °C)	Less than 0.05% FSR ± ½ LSB (Gain 1X) Less than 0.07% FSR ± ½ LSB (Gain 2X, 4X, 8X) [Includes 3 sigma noise, linearity, offset gain and dynamic response errors]
Input Impedance —	680 ohms (power off) Greater than 100 megaohms (power on)
Input Current —	0 to 20 ma (with 250 ohm user installed resistors)
Common Mode —	
Voltage	±10.24 V maximum (signal and common mode)
Rejection	−60 db (differential input) at source impedance: Balanced — less than 5000 ohms Unbalanced — less than 1000 ohms
Crosstalk —	−86 db at 10 KHz
Overvoltage Protect —	±28 VDC, AC peak
Temperature Coefficient —	Less than 0.003% FSR/ °C
Monotonicity —	Guaranteed over the operating temperature range
External Trigger —	±4 V for 200 ns (min) with ≤50 ns rise time
Pacer Clock —	Crystal controlled, 0.05% accuracy Divider range $\frac{1024}{2^n}$ ms (n = 0 through 10)
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
Connectors —	
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Analog	One 50 contact input double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH312125 or equivalent One 60 contact auxiliary double-sided edge connector on 0.1 inch centers Recommended mating connectors: CDC VPB01B30A00A2 AMP PES-14559 TIH 311130 One 50 contact input expansion double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH 312113 or equivalent

Power — +5V, 2.3A
If Auxiliary Power is used:
±15VDC ±5%, 150ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

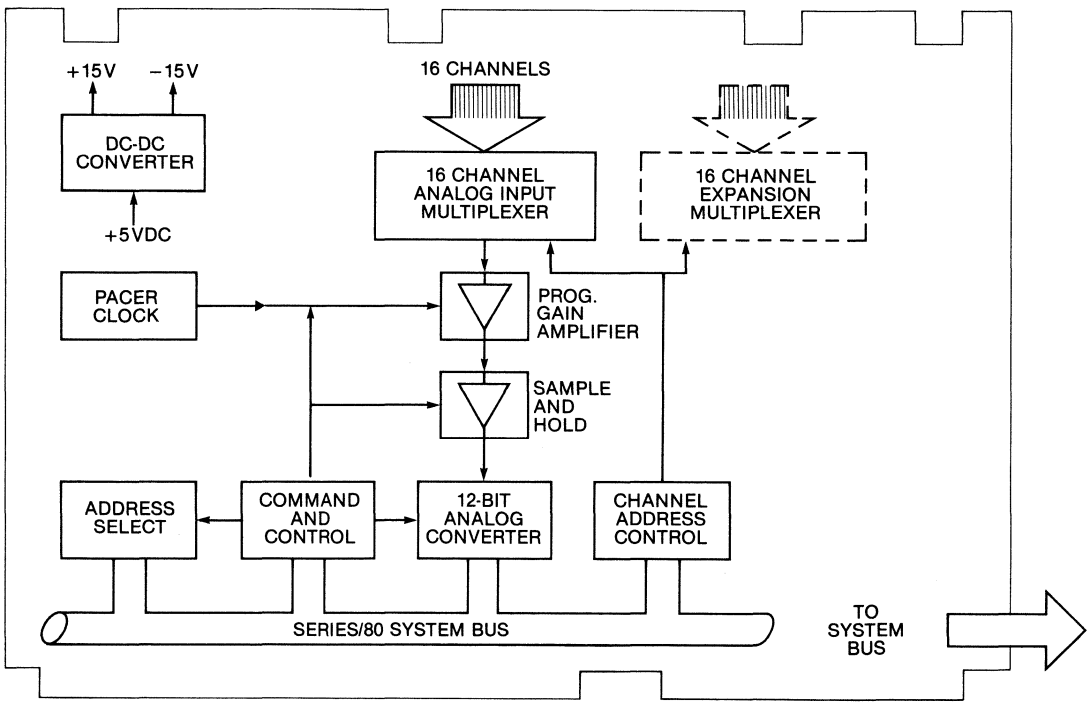
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	20 oz.	(567 g)

Order Information

BLC-711	Analog Input Board Includes 16 single-ended or 8 differential analog input channels, manual and diagnostic test program in paper tape media

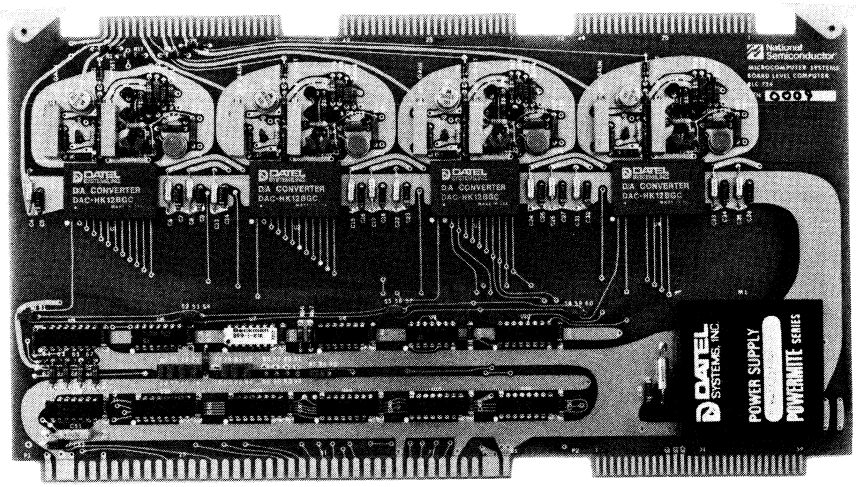
Documentation

420305649-001	BLC-711 and BLC-732 Analog Input and Combination Input/Output Board Hardware Reference Manual



BLC-711 Diagram

BLC-724
Analog Output Board



- **Application Flexibility**
  - Four independent channels
  - Unipolar and bipolar operation
  - Voltage and current mode outputs
- **Fast 3 Microsecond Settling Time**
- **12-bit Resolution with 0.05% Accuracy for High Overall Accuracy**
- **Plug-replacement for SBC-724**

Product Overview

The BLC-724 Analog Output Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation, control and analog display applications.

Compatible with the Series/80 system bus, the board provides the logic functions necessary to convert digital data to analog output signals. Four independently controlled channels are provided, each with 12-bit resolution.

Analog outputs may be unipolar or bipolar, thus providing application flexibility. Channel output is from 0 to ±10 volts or may be employed in a 4 to 20 milliamp current loop mode.

The BLC-724 is a plug-compatible replacement for the Intel SBC-724.

Functional Description

Standard Series/80 instructions control analog output. Memory mapped I/O simplifies the programming task by permitting the transfer of output data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O a segment of 8 contiguous addresses is predefined by the user and set on the board via jumpers. These addresses may be on any 8 byte boundary within the 64K bytes of available address space. Analog output starts when the most significant byte (second byte) of the Write command is transferred to the digital to analog channel converter. The control parameter configuration is illustrated in Figure 1. Memory inhibit logic prevents address contention for memory mapped I/O addresses.

7	6	5	4	3	2	1	0
Data 11 (MSB)	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4

Second Byte (MS Byte)

7	6	5	4	3	2	1	0
Data 3	Data 2	Data 1	Data 0 (LSB)	0	0	0	0

First Byte (LS Byte)

Address	Write Command Function	Channel
Base + 0	Load LS Byte	0
Base + 1	Load MS Byte	0
Base + 2	Load LS Byte	1
Base + 3	Load MS Byte	1
Base + 4	Load LS Byte	2
Base + 5	Load MS Byte	2
Base + 6	Load LS Byte	3
Base + 7	Load MS Byte	3

Figure 1. Analog Output Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5 VDC power input to the ±15 VDC required by the analog generating circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-724 to allow testing and calibration of the analog output channels. Calibration is recommended when a channel range jumper is set.

Specifications

General

Number of Channels — 4 non-isolated

Channel Resolution — 12 bits including sign

Slew Rate — 10 volts per microsecond (no external capacitance)

Settling Time — 3 microseconds to ½ LSB (5 volt step change)

Accuracy — 0.05% FSR at 25°C (includes linearity and noise)

Monotonicity — Guaranteed over operating temperature range

Voltage Mode Output Characteristics

Full Scale Range (Jumper Select) — 0 to +5V, 0 to +10V, ±5V, ±10V

Output Current — ±5ma at ±10V

Output Impedance — 0.05 ohms

Output Capacitance — 1000pf maximum

Current Mode Output Characteristics

Full Scale Range — 4 to 20ma current loop, unipolar (requires external loop voltage of 15 to 30VDC)

Load Impedance — 500 ohms maximum

Other

System Bus Interface — Data, address and command signals are TRI-STATE™ TTL compatible

Connectors —

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — One 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
CDC VPB01B30A002
AMP PES-14559
TIH 31110

Analog Output — One 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-000,
TIH 312125, or equivalent

Power — +5V, 1.5A

If Auxiliary Power is used:
±15VDC ±5%, 150ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

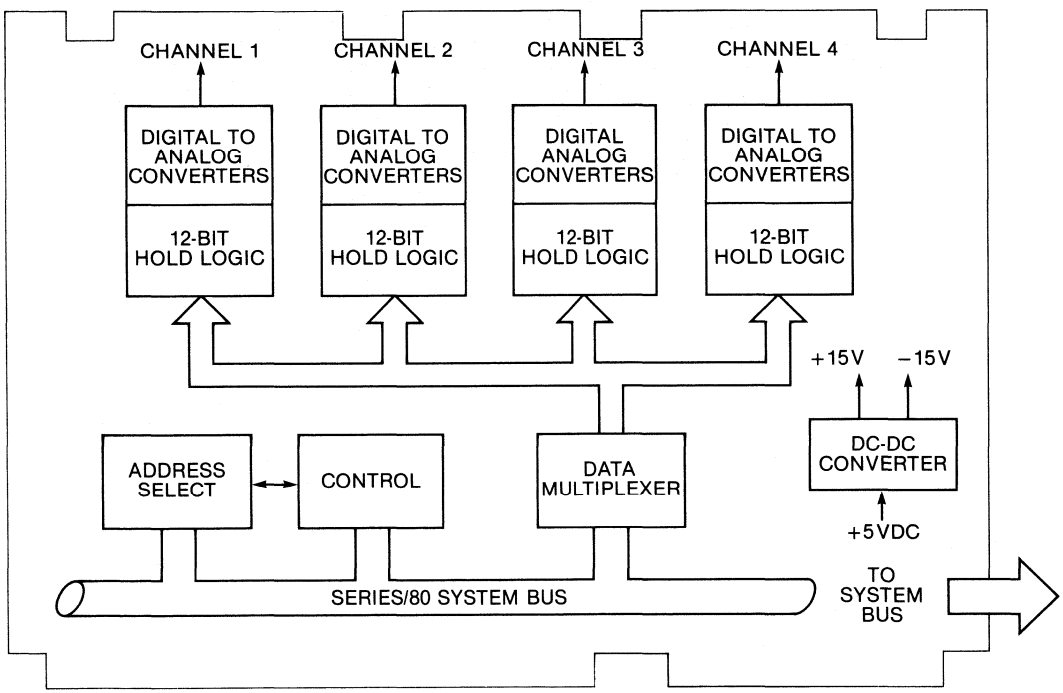
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	18 oz.	(510.3 g)

Order Information

BLC-724	Analog Output Board Includes 4 independent high level analog output channels, manual and diagnostic test program in paper tape media.

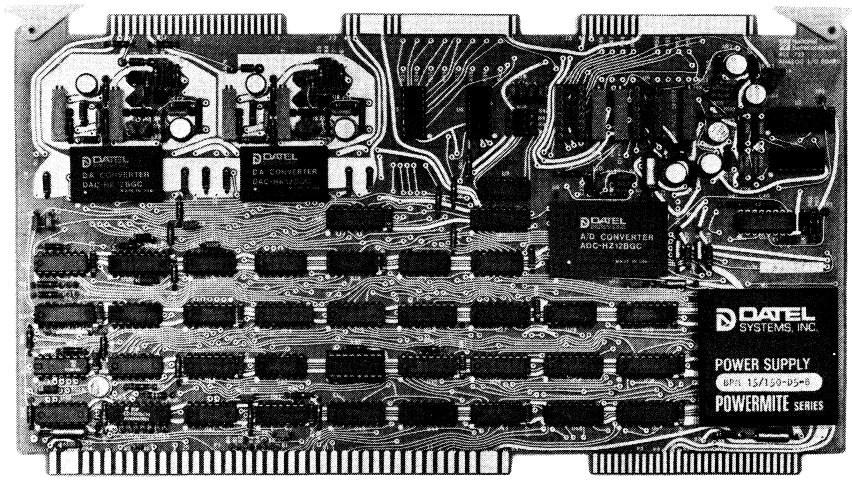
Documentation

420305647-001	BLC-724 Analog Output Board Hardware Reference Manual



BLC-724 Diagram

BLC-732
Combination Analog Input/Output Board



- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - 2 output channels
  - Unipolar and bipolar operation
  - Voltage and current mode inputs and outputs
  - Sequential, random and single channel scan modes
- **50 KHz Sample Rate Permits Use in Wide Range of Applications**
- **12-bit Resolution with 0.05% Overall Input and 0.05% Output Accuracy for Precise Measurements**
- **On-board Pacer Clock or External Synchronization of Sampling for System Flexibility**
- **Programmable Gain Amplifier Accommodates Wide Range of Systems**
- **Plug-replacement for SBC-732**

Product Overview

The BLC-732 Combination Analog Input/Output Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process control applications.

The BLC-732 provides multiple analog input and output capability. The input function allows sampling of analog data at a rate of 50,000 samples per second and storage of equivalent digital values for subsequent processing. The BLC-732 is equipped with sample and hold circuitry, and accuracy of conversion is assured by holding the input sample constant until conversion is completed. The output function permits digital data conversion of 0 to ±10 volts analog in unipolar or bipolar output form.

Analog inputs may be sampled in random, sequential or single channel repetitive mode. The board contains high resolution 12-bit analog converters for input and output, 16 single-ended or 8 differential input channels, 2 output channels, programmable gain input amplifier and the sample and hold function. The analog input capacity is expandable to 32 single-ended or 16 differential channels.

The BLC-732 is a plug-compatible replacement for Intel's SBC-732.

Functional Description

Standard Series/80 instructions control analog input and output. Memory mapped I/O simplifies the programming task by permitting the transfer of data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O, a segment of 16 contiguous addresses is predefined by the user and set on the board via jumpers. These addresses may be on any even 16 byte boundary within the 64K bytes of available address space. If these addresses overlay system memory addresses, memory inhibit logic prevents address contention for memory mapped I/O addresses.

Analog Input

Analog to digital (A/D) conversion is initiated by a Write command to the Multiplexer Address Register (MAR). The bit pattern of the MAR specifies the gain and the specific channel to be converted. The Command Register (CR) is then loaded with a bit pattern that enables conversion and the desired interrupts. Bits in the Command Register also specify pacer clock/external trigger, clearing, the board busy bit, and enabling sequential scan.

If the sequential scan feature is enabled, input channels will be sequentially converted until the channel address in the Last Channel Register (LCR) is reached.

Data sent to the Command Register can be read back by issuing a Read command to the Status Register (SR). In addition to verifying the last command word sent to the Command Register, the status also signifies that the last channel has been reached.

After analog conversion is complete, the corresponding digital data value is read from the converter register. The first byte contains the low order 4 bits (bits 0 to 3) of the digital representation; the second byte contains the 8 high order bits (bits 4 to 11).

The selected analog input is applied to the A/D converter through a software controlled programmable gain amplifier which provides gains of X1, X2, X4, or X8, and a sample and hold amplifier. With the A/D converter jumper selected for +5V, +10V, ±5V, or ±10V full scale input voltages, the gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable Gain Full Scale Values

Gain Selected	Voltage Range Selection			
	+5V	+10V	±5V	±10V
X1	+5V	+10V	±5V	±10V
X2	+2.5V	+5V	±2.5V	±5V
X4	+1.25V	+2.5V	±1.25V	±2.5V
X8	+0.625V	+1.25V	±0.625V	±1.25V

Sampling is controlled in one of three ways: by program instruction (writing the multiplexer address to an analog input channel), by an internal sample timer (pacer clock), or by external event synchronization (external trigger). The pacer clock may be jumper configured to provide timing intervals from 975 microseconds to 1 second.

Interrupts to the system CPU may be generated upon completion of either a channel sample conversion or a sequential channel scan. This relieves the system CPU of continuous status scanning.

The analog input control parameters are illustrated in Figure 1.

7	6	5	4	3	2	1	0
Gain Select	Gain Select	Not Used	2^4	2^3	2^2	2^1	2^0
			Channel Select				

	Bit	
Gain	7	6
X1	0	0
X2	0	1
X4	1	0
X8	1	1

a. Multiplexer Address and Gain Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Not Used	2^4	2^3	2^2	2^1	2^0
			Last Channel Address				

b. Last Channel Sampled Address Format

7	6	5	4	3	2	1	0
Not Used	Not Used	End of Conv. Intrpt	End of Scan Intrpt	Clear Busy	Exit Trig Enable	Auto Incr Enable	Start/ Stop

c. Command Register Byte Format

7	6	5	4	3	2	1	0
Conv. Done	Scan Done	End of Conv. Intrpt	End of Scan Intrpt	Busy	Exit Trig Enabl	Auto Incr Enabl	Start/ Stop

d. Status Register Byte Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Clear End of Conv. Intrpt	Clear End of Scan Intrpt	Clear Pacer Clock	Not Used	Not Used	Not Used

e. Clear Interrupts Format

Address	Write Command Description
Base + 0	Load Command Register (CR)
Base + 1	Load Multiplexer Address Register (MAR)
Base + 2	Load Last Channel Register (LCR)
Base + 3	Clear Interrupts

Address	Read Command Description
Base + 0	Read Status Register (SR)
Base + 1	Read Multiplexer Address Register (MAR)
Base + 4	Read LS Byte, A/D (ADCR)
Base + 5	Read MS Byte, A/D (ADCR)

f. Memory Mapped Addressing

Figure 1. Analog Control Parameters

Analog Output

The two independent analog outputs may be unipolar or bipolar and provide outputs from 0 to +5V, +10V, ±5V and ±10V using on-board jumper select options. Current mode output from 4 to 20 milliamps may be implemented by adding discrete resistors with the mode jumper set for unipolar operation. The current mode requires an external loop voltage of +15 to +30 volts. +15 volts may be derived from the on-board DC to DC converter.

The analog output is available when the most significant byte (the second byte) of the Write Command is transferred to the digital to analog channel hold register. Figure 2 illustrates the output parameters.

7	6	5	4	3	2	1	0
Data 11 (MSB)	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4

Second Byte (MS Byte)

7	6	5	4	3	2	1	0
Data 3	Data 2	Data 1	Data 0 (LSB)	0	0	0	0

First Byte (LS Byte)

Address	Write Command Description	Output Channel
Base + 8	Load LS Byte	0
Base + 9	Load MS Byte	0
Base + A	Load LS Byte	1
Base + B	Load MS Byte	1

Figure 2. Analog Output Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5VDC power input to the ±15VDC required by analog circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-732 to allow testing and calibration of the analog circuits. Calibration is recommended when a channel full scale range jumper is set.

Specifications

Analog Input

Scan Mode — Sequential; Random; Single Channel Repeat

Channels — 16 single-ended or 8 differential

Channel Resolution — 12 bits

Full Scale Range Volts — 0 to +0.625; +1.25; +2.5; +5
0 to +1.25; +2.5; +5; +10
±0.625; ±1.25; ±2.5; ±5
±1.25; ±2.5; ±5; ±10

Programmable Gain — X1, X2, X4, X8

Sample and Hold —
- Aperture Time — Less than 100 nanoseconds
- Uncertainty Time — 20 nanoseconds
- Acquisition — 8 microseconds

Throughput Rate — 24 KHz

A/D Conversion Speed — 50 KHz

Overall Accuracy — (25 °C)
Less than 0.05% FSR ± ½ LSB (Gain 1X)
Less than 0.07% FSR ± ½ LSB (Gain 2X, 4X, 8X)
[Includes 3 sigma noise, linearity, offset gain and dynamic response errors]

Input Impedance — 680 ohms (power off)
Greater than 100 megaohms (power on)

Input Current — 0 to 20 ma (with 250 ohm user installed resistors)

Common Mode —
- Voltage — ±10.24V maximum (signal and common mode)
- Rejection — −60 db (differential input) at source impedance
  Balanced — less than 5000 ohms
  Unbalanced — less than 1000 ohms

Crosstalk — −86 db at 10 KHz

Overvoltage Protect — ±28 VDC, AC peak

Temperature Coefficient — Less than 0.003% FSR/ °C

Monotonicity — Guaranteed over the operating temperature range

External Trigger — ±4V for 200ns (min) with ≤50ns rise time

Pacer Clock — Crystal controlled, 0.05% accuracy
Divider range $\frac{1024}{2^n}$ ms
(n = 0 through 10)

Analog Outputs

Channels — 2 non-isolated

Channel Resolution — 12 bits including sign

Slew Rate — 10 volts per microsecond (no external capacitance)

Settling Time — 4 microseconds to ½ LSB

Accuracy — 0.05% FSR at 25°C (includes linearity and noise)

Temperature Coefficient — 0.005% FSR/°C

Monotonicity — Guaranteed over operating temperature range

Other

Voltage Mode Output Characteristics —

Full Scale Range (Jumper select)	0 to +5V 0 to +10V 0 to ±5V 0 to ±10V 4 to 20ma
Output Current	±5ma at ±10V
Output Impedance	0.05 ohms
Output Capacitance	1000pf maximum

Current Mode Output Characteristics —

Full Scale Range	4 to 20ma current loop, unipolar (requires external loop voltage of 15 to 30 VDC)
Load Impedance	500 ohms maximum

System Bus Interface — Data, address and command signals are TRI-STATE™ TTL compatible

Connectors —

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Analog — One 50 contact input double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
3M 3415-000, TIH312125

One 60 contact auxiliary double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
CDC VPB01B30A00A2
AMP PES-14559
TIH 311130

One 50 contact input expansion double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
3M 3415-000, TIH 312113 or equivalent

One 50 contact output double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
3M 3415-000, TIH 312125 or equivalent

Power — +5V, 2.5A

If Auxiliary Power is used:
±15VDC ±5%, 150ma

Environmental — Temperature 0° to 55°C

Humidity 0 to 90% non-condensing

Physical —

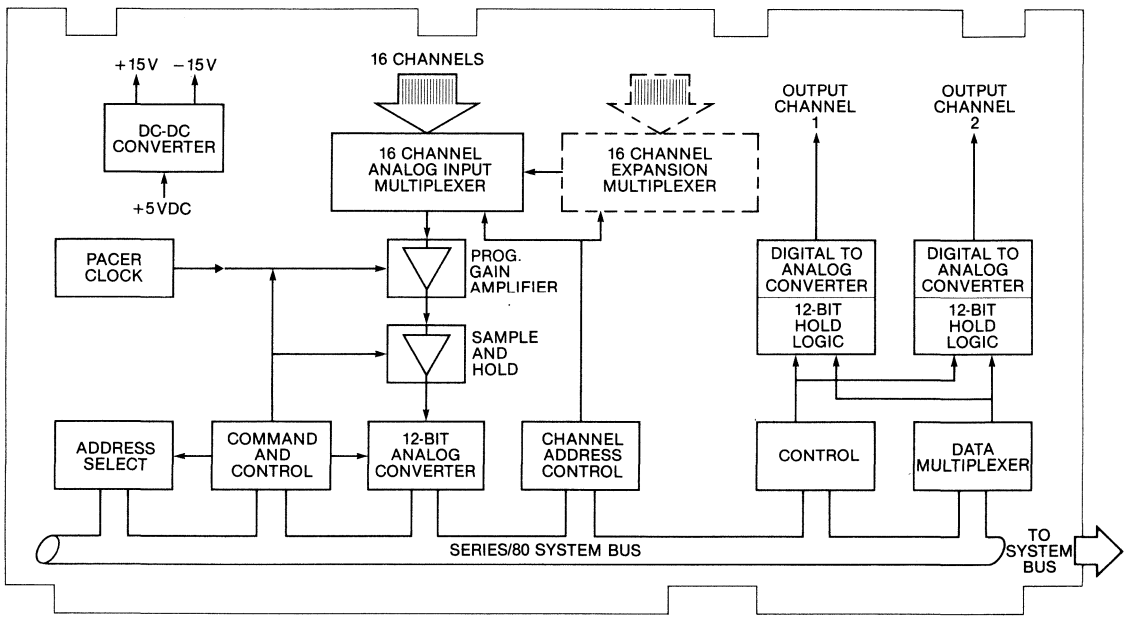
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	18 oz.	(510.3 g)

Order Information

BLC-732 — Combination Analog I/O Board Includes 16 single-ended or 8 differential analog input channels and 2 analog output channels, manual and diagnostic test program in paper tape media

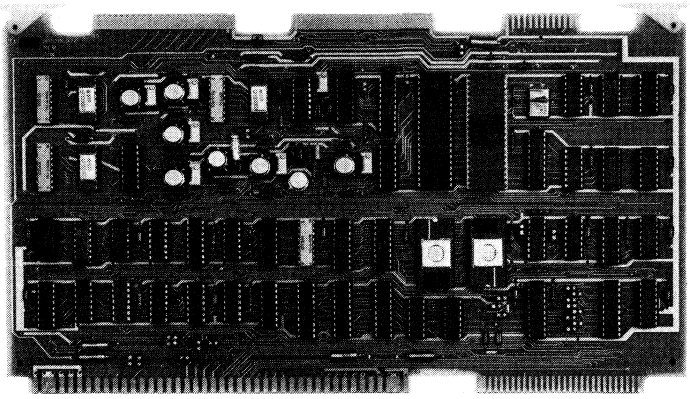
Documentation

420305649-001 — BLC-711 and BLC-732 Analog Input and Combination Input/Output Board Hardware Reference Manual



BLC-732 Diagram

BLC-8715
Intelligent Analog I/O Board



- **Intelligent Analog Input with Stand-Alone Measurement and Control Capability**
- **Low Cost Computing Power**
  - 8085 CPU
  - 1K static RAM
  - Up to 4K ROM/PROM
  - Memory-mapped 256 byte RAM communication/control "MAILBOX"
  - 4 interrrupt levels
- **22 Channels Programmable Digital I/O**
- **RS232C Serial Interface**
- **Programmable 14-Bit Counter/Timer**
- **Analog Application Flexibility**
  - 16 single-ended/8 differential channels software configurable in any mix.
  - Bipolar capability from ±400 microvolts to ±5 volts.
  - All seven available gains from 1 to 100 software programmable.
  - 8-bit, 8-microsecond ADC conversion. Dynamic range expansion to >12 bits using auto-range techniques.
  - Scan modes software configurable.
  - 25kHz data throughput.
  - 4mHz bandwidth Bifet™ instrumentation amplifiers.
  - Analog measurement sequence after channel selection to end-of-conversion hardware controlled, freeing CPU for other tasks.
  - ±1 LSB overall analog accuracy, including quantizing and worst-cased for all error sources.
- **Firmware Monitor available with CPU programming, analog configuration, analog scanning, and calibration features**
- **Compatible with All Series/80 Boards and Card Cages**

Product Overview

The BLC-8715 is a self-contained low-cost stand-alone computer with flexible analog measurement and digital I/O capability. The BLC-8715 extends the Series/80 family of microcomputer products into a wider variety of instrumentation and industrial applications by providing dedicated distributed processing capability in a single board.

The analog capability of the BLC-8715 provides for multiple inputs. The analog input functions allow an input sampling rate of 25kHz, and subsequent processing and storage may be performed on-board. The BLC-8715 is equipped with sample and hold circuitry. Accuracy of conversion is assured by dedicated logic providing proper sampling and

holding intervals. Analog inputs may be sampled in any mix of random, sequential and repetitive modes, under on-board computer control. The board contains an 8-bit analog converter, 16 single-ended or 8 differential channels, programmable gain amplifier, and sample hold functions.

The BLC-8715 is also a complete computer including a CPU, serial communications interface, 22 parallel I/O, 1K-bytes private static random access memory, sockets to accept up to 4 K-bytes of read only memory, a 14 bit counter/timer, a system clock, and an additional 256 bytes of RAM accessible by the local CPU, or a MULTIBUS host CPU, mappable over the system 64 K-byte address space.

The BLC-8715 is configured as a MULTIBUS slave and may be interrrupt or status driven by a MULTIBUS host, communicating through its 256 byte dual access mailbox memory.

Functional Description

Central Processor

The CPU is an 8085A which has 100% software compatibility with the 8080A. The advanced features of the 8085A chip set are utilized to provide a system clock, vectored interrupts, serial I/O, memory and parallel I/O.

Memory

The BLC-8715 provides 1024 bytes of private RAM implemented with MM2114 modules. Private RAM is mapped from 2000_H to $23FF_H$.

Sockets and jumper options are provided to implement up to 2 K-bytes of EPROM with 2708s or 4 K-bytes with 2716s, or their ROM equivalents. ROM/PROM addressing is defined from 0000_H to limits set by the type and quantity of ROM/PROM used.

The BLC-8715 also provides 256 bytes of RAM accessible by either the BLC-8715 CPU or a MULTIBUS host for communication and control. This "mailbox" is addressed from BASE + 00_H to BASE + FF_H, where BASE is set by user selectable jumpers on 256 byte boundaries. Means are provided to permit the local CPU to determine the BASE address.

Parallel I/O

22 parallel I/O lines are provided by the I/O section of an 8155. Using standard 8080/8085 instructions, the 22 lines may be configured into a wide variety of unidirectional, bidirectional, and interrupt/ status driven modes.

Serial I/O

The unique serial SID and SOD pins of the 8085 are interfaced to the outside world via RS232 drivers. Using software techniques only, or in combination with the timer section of the 8155, baud rates up to 9600 may be implemented. Power from the BLC-8715 is made available to the 26 contact J1 card edge to support the BLC-530 TTY adapter.

Interval Timer

A 14-bit programmable timer is made available as part of an 8155. The timer out pulse is default jumpered to interrupt RST 7.5, which is edge latched by the CPU and may be acknowledged and reset by software.

Interrupt System

4 interrupt levels are supported by the BLC 8715.

Interrupt Level	Priority
TRAP	1 (highest)
RST 7.5	2
RST 6.5	3
RST 5.5	4

Trap is a non-maskable interrupt and is normally disabled by a jumper to GND but may be jumpered to pin 19 of P2 for power-fail shut down purposes or similar catastrophic events.

RST 7.5 is an edge sensitive, latched, maskable interrupt which is normally jumpered to the timer output.

RST 6.5 is a level sensitive, maskable interrupt which is normally jumpered to the ADC end-of-conversion (EOC) latch. The EOC latch is reset whenever the ADC output register is read by the CPU.

RST 5.5 is a level sensitive, maskable interrupt which is normally disabled, but may be connected to any of various sources.

The 8155 parallel port handshake lines are brought to the interrupt jumper matrix to utilize any of the available interrupt levels as desired.

MULTIBUS interrupts, INT0/ — INT7/, are brought to the interrupt matrix to utilize any of the available interrupt levels.

Analog Input

A flexible local CPU interface to the analog measurement control hardware is provided via 4

unique I/O instructions. These instructions provide the following functions:

I/O ADDRESS	I/O OPERATION	FUNCTION
07_H to $F7_H$	Read	• Starts measurement sequence • Selects input channel (High Nibble = Input Channel I.D.) • Causes a gain/ configuration register to output 3 bits to gain selector switch and 1 bit to configuration (single/differential) selector switch • Sampling interval & hold timing through end of conversion interrupt generation is initiated by this instruction.
06_H	Read	• Places ADC output into CPU accumulator • Resets measurement control logic • Resets EOC interrupt • Resets base address interrupt when used to retrieve base address on CPU initialization
06_H	Write	• Sets an interrupt which may be used to generate an interrupt to a MULTIBUS host. This is automatically cleared when host accesses BLC-8715
07_H to $F7_H$	Write	• Writes lower nibble of CPU accumulator to the 16 × 4 bit gain/ configuration register. High nibble of I/O address corresponds to each input channel I.D.

Analog input scan modes (sequential, random, repetitive) may be simply achieved in software by configuring the sequence of I/O reads. The BLC-8915 Firmware Monitor provides a convenient method of passing the desired scan parameters to the CPU via the 256 byte mailbox.

Firmware Monitor

The BLC-8915 Monitor provides the following functions:

- Serial I/O operator interface routine via CRT/Keyboard
- Initialization of all BLC-8715 hardware
- Direct user through calibration, test, and measurement scan
- Provide programming routines (modify and display memory, modify and display CPU registers, initiation of user program, insert, breakpoint, single step, and read and dump paper tape)

The monitor makes use of the memory mapped mailbox to provide a host/stand-alone software interface to transfer channel configuration, scan control, command, and data to or from the resident firmware. The address of the mailbox is from BASE + 00_F to BASE + FF_H, where BASE is user selectable jumper code relocating the mailbox anywhere in the 65K address range on the 256 byte boundaries.

BASE + 0 is dedicated as a command register. After a write operation to this location, by either a host or the local CPU, the analog measurement is started. The mailbox is defined in Table A for use by the BLC-8915 Monitor, and represents one of many possibilities for providing a flexible software information and control interface.

A. Dual Access Register

Host operation options are specified in the following table. For stand-alone operation, user BLC-8715 software could initialize the table as desired. The BLC-8915 Monitor provides default values of sequential scan, no skips, stop scan after one cycle, scan all channels with gain of 1, and single-ended channel configuration. Under monitor control, a user may initialize the table, then use the monitor "A" command to commence the scan.

Table A

Address	Name	Operation
Base + 0_H	Command	Write
Base + 1_H	Status	Read
Base + 2_H	Acknowledge	Read/Write
Base + 3_H	Scan Parameter	Write
Base + 4_H to Base + 15_H	User Defined	User Defined
Base + 16_H	Start Scan	Write
Base + 17_H	End Scan	Write
Base + 18_H to Base + 27_H	Configuration	Write
Base + 28_H to Base + 37_H	Data	Read
Base + 38_H to Base + FF_H	User Defined	User Defined

B. Command Register (Base + 0_H)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	EOS INT.

If bit 0 is set, an interrupt to the Series/80 bus is generated after one scan cycle. After a write to this register, a scan sequence is started.

C. Status Register (Base + 1_H)

This register may be user defined to post status. It is not used by the BLC-8915 Monitor.

D. Acknowledge Register (Base + 2_H)

Useful as a host/slave software in continuous scan operation. The BLC-8715 writes FF_H after each scan. The BLC-8715 can then monitor this register until host has read the scan data and cleared this register before the BLC-8715 starts its next scan sequence.

E. Scan Parameter Register (Base + 3_H)

7	6	5	4	3	2	1	0
X	X	X	Single or Repetitive Scan	No. of Channels Skipped			

If skip scan is specified in the command register, the program looks up the number of channels to skip from this register, after previously looking up the starting channel address.

F. User Defined (Base + 4_H to Base + 15_H)

These may be used to expand scan control registers, HI/LO alarm limits for each channel, or additional status conditions.

G. Start Scan Register (Base + 16_H)

7	6	5	4	3	2	1	0
Relative Base Address of Start of Scan Channel (18_H to 27_H)							

H. End Scan Register (Base + 17_H)

7	6	5	4	3	2	1	0
Relative Base Address of End of Scan Channel (18_H to 27_H)							

I. Configuration Registers (Base + 18_H to Base + 27_H)

7	6	5	4	3	2	1	0
Channel No.				Single/ Differential	Gain		

0	0	1	X1
0	1	0	X2
0	1	1	X5
1	0	0	X10
1	0	1	X20
1	1	0	X50
1	1	1	X100

In a scan mode, channel selection is sequential from contents of Base + 18_H to Base + 27_H in ascending order. Random scan is achieved by writing the random sequence desired.

Differential channels consist of paired single-ended channel numbers N and N + 8, where N = 0 to 7. Only the address of the upper channel of a differential pair need be specified for differential selection.

J. Data Registers (Base + 28_H to Base + 37_H)

7	6	5	4	3	2	1	0
ADC OUTPUT							

The monitor simply writes the output corresponding to each channel specified by the Configuration Register to the corresponding Data Registers. The BLC-8715 provides a jumper to obtain either 2's complement or offset binary format.

Specifications

Microprocessor

CPU — 8085A

Instruction — 8, 16, or 24 Bits

Data — 8 Bits

Cycle Time — 2.00 microsecond for fastest instruction, i.e. 4 clock cycles

System Clock — 2.00mHz ± 0.1%

Memory

RAM — 1024 Bytes, private
256 Bytes, dual access

ROM — Sockets for up to 4k Bytes

Parallel I/O — 22 programmable lines (three 8155 ports)

Serial I/O — SID and SOD functions of 8085 CPU used for serial communications controlled by software through RIM and SIM instructions. RS-232 and TTL interfaces. TTY interface via BLC 530 adapter.

Interrupts — Four-level interrupts routed to CPU. Each interrupt automatically refers to a unique address location.

Timer — 14-bit programmable timer 125.0kHz ± 0.1% clock input

Analog Input

Scan Mode —	On-board programmable (sequential, random, repeat, mixed)
Channels —	16 single-ended or 8 differential (software configurable in any mix)
Channel Resolution —	8-bit 2's complement or offset binary. Dynamic range of A/D converter expanded to greater than 12 bits with auto ranging capability via programmable gains.
Full Scale Range —	±(0.05, 0.10, 0.25, 0.5, 1.0, 2.5, 5.0) volts
Programmable Gain —	X1, X2, X5, X10, X20, X50, X100
Sample Time —	Default jumpered to 32 microseconds to insure 12-bit accuracy @ X 100 gain. Rejumperable to 2 microseconds, in steps.
Input Leakage —	< 10nA @ 25°C
Current —	< 60nA, 0-70°C
Input Resistance —	2 Kohms, power off > 100 Megohms, power-on
Input Capacitance —	< 100pF
Channel Crosstalk —	< 80dB @ 200Hz
Sample and Hold Feed Through —	< 80dB @ 200Hz
Common-Mode Rejection —	> 60dB @ 1 kohm source unbalance
Common-Mode Voltage —	±5 volts, max (signal + common mode)
Input Over Voltage Protection —	±30 volts, peak
Overall Accuracy —	6 months, 15°C to 35°C, ±(0.4% RDG + 1 LSB)
Accuracy Tempco —	0 to 15°C & 35°C to 50°C, ±(0.01% RDG + 0.01% Range)/°C
Monotonicity —	Guaranteed, 0-70°C
System Interface —	MULTIBUS™ compatible memory-mapped slave

Connectors

System Bus —	86 contact double-sided card edge connector on 0.156 inch centers
Auxilliary Bus —	60 contact double-sided card edge connector on 0.1 inch centers
Parallel I/O — and Analog Inputs	50 contact double-sided card edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26 contact double-sided card edge connector on 0.1 inch centers Recommended mating connector: 3M 3462-0001 AMP 1-583715-1

Power	**VDC**	**Max Current**
	+5	2A
	−5	100mA with 2708 EPROM
	+12	250mA
	−12	250mA

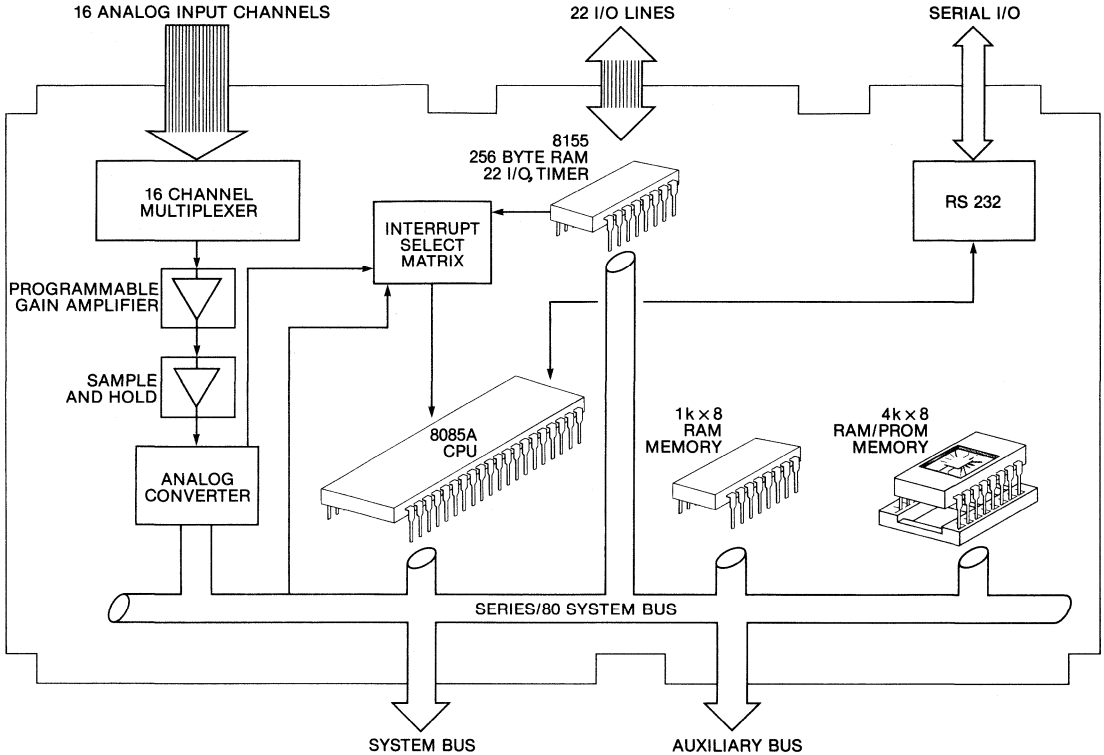
Environmental	Temperature 0-70°
	Humidity 0-90% RH, non condensing
Physical	Height 6.75 in (17.15 cm)
	Width 12.00 in (30.48 cm)
	Depth 5 in (12.7 cm)
	Weight 14 oz (397 gm)

Order Information

BLC-8715	Series 80 Intelligent Analog Board includes CPU, 1KB static RAM, sockets for up to 4KB ROM, 22 parallel digital I/O, serial I/O interface, timer, and 16 single-ended or 8 differential channel analog processing capability.
BLC-8915	BLC-8715 Monitor provides CPU programming, analog configuration, analog scanning, analog measurement, and analog calibration functions.

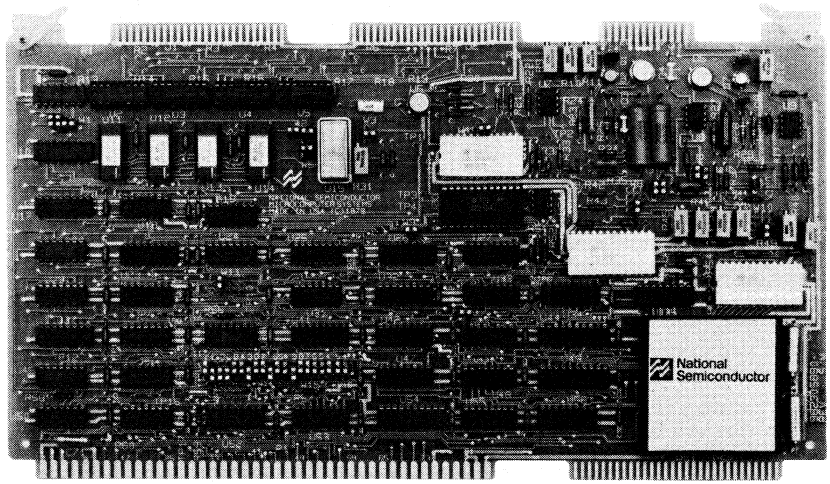
Documentation

420305927-001	BLC-8715 Intelligent Analog Board Hardware Reference Manual



BLC-8715 Diagram

BLC-8737
Analog Input/Output Board With Memory



- **Mailbox Bus Interface**
  - Latest data from all channels stored on-board
  - Gains need be set only once
  - Simple memory reference instructions to read data or set gains
- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - 2 output channels
  - Provisions for 4-20ma inputs and outputs
  - Programmable gain amplifier
  - Sequential scan or CPU-driven selected channel conversions
  - Input protection up to 125VAC
- **12-Bit Resolution With ±0.05% Overall Input and Output Accuracy**
- **4-20ma True Current Sourcing Output Channels Permit Grounded Loads**
- **Single 5V Power Required**

Product Overview

The BLC-8737 analog I/O Board with memory extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process-control applications, yet minimizes the data interfacing software because of the on-card memory. Multiple analog input and output capability is provided.

The BLC-8737 makes each input channel appear to be a RAM address. Data is read by a single memory-read instruction at normal memory speeds. Writing into that address once will set the gain on that channel until reset to a different gain by a subsequent write (gain) instruction.

Analog inputs are automatically sampled in sequential repetitive mode. However, a gain-set write instruction will re-start the scan at that channel. This mode, together with an interrupt output, allows random or equivalent single-channel operation when desired. The throughput rate is 8500 channels/second, and is adequate for most process/instrumentation systems with data bandwidth to 100/200/400 Hz on each of 32/16/8 channels.

The input circuitry contains 16 single-ended or 8 differential-channel multiplexers, input protection on each channel, a fast-settling differential (instrumentation) amplifier with software programmable gain, sample-and-hold amplifier, a 12-bit analog-to-digital converter, voltage reference, gain-program memory, and 32-channel data memory. The input may be expanded to 32 single-ended or 16 differential channels.

The output circuitry contains two 12-bit digital-to-analog converters with latched input registers, a precision voltage reference with offsetting circuitry, and two 4-20ma voltage-to-current converters with true current sourcing to permit grounded loads.

Input channels are memory mapped to any contiguous block of addresses which are jumper selected beginning with an even address. Output channels are memory mapped anywhere else within the same 2K block as the input channels. RAM and ROM inhibit signals are provided, should the I/O card address overlap installed memory.

Functional Description

Standard Series/80 instructions control analog input and output. Memory mapped I/O and single memory-reference read and write instructions greatly simplify the programming task and reduce computer timing load compared with other analog I/O systems.

With memory mapped I/O, a segment of 32 contiguous addresses (16 double-byte locations) is predefined for input channels, and set by movable jumpers on the board. These addresses may be on any given 32-byte boundary within the 64K bytes of available address space. These addresses overlay system memory address functions with memory inhibit logic to prevent address contention for memory-mapped I/O addresses. Output channels share the same six most significant address bits with input addresses, however, they may be jumper selected to any other block of 16 locations within the same 2K space occupied by the input channels.

Analog Input

The card normally operates in a sequential scan mode with a 118 microsecond period devoted to each channel. This allows settling time for the multiplexer, instrumentation amplifier, and S/H amplifier ADC conversion time and data load time for on-card RAM. The BLC-8737 is always in operation, loading RAM with latest data for each channel and updating RAM on each succeeding scan. The data is read with a memory-read instruction (LHLD). Input data appears as 12 bits, right justified in a 16-bit data format. Bipolar data includes extended sign.

If channel data must be known to be more current than 2 milliseconds, the random access feature may be employed. To use this feature it is only necessary to re-write the gain instruction for the desired channel. A gain-set instruction will reset the channel address counter to the addressed channel, and will initiate a data acquisition/conversion cycle. At completion of conversion, an interrupt will signal when current data may be read as outlined above. The interrupt may be set to any, or none, of the eight bus interrupt lines.

The selected analog input is applied to the A/D converter through a software controlled programmable-gain amplifier which provides gains of 1,2,5, or 10, and a sample-and-hold amplifier. A set of movable jumpers allow additional gain multiples of 1, 4 or 10 applied to the above gains. With the ADC jumper selected for +10.24 or ±10.24 full-scale input voltage, the variable gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable-Gain Full-Scale Values

Gain Selected			
Software	Jumper	Unipolar	Bipolar Selection
1		+10.24	±10.24
2		+ 5.12	+ 5.12
5	1	+ 2.048	+ 2.048
10		+ 1.024	+ 1.024
1		+ 2.56	± 2.56
2		+ 1.28	± 1.28
5	4	+ 0.512	± 0.512
10		+ 0.256	± 0.256
1		+ 1.024	± 1.024
2		+ 0.512	± 0.512
5	10	+ 0.2048	± 0.2048
10		+ 0.1024	± 0.1024

The only analog input control parameter is the gain setting for each channel. After system initialization, gain must be set for every channel. Part of a post-initialization or system start-up program will be a series of gain-set memory-write instructions, one to each channel address. A two-bit gain word may be written into either byte of the addresses assigned to the input channels. The gain select words are described in Table II.

Table II Gain-Set Data Word

Gain	Data Word
1	(MSB) X X X X X X 1 1
2	X X X X X X 1 0
5	X X X X X X 0 1
10	X X X X X X 0 0

Analog Output

Two independent analog outputs may be unipolar or bipolar, and provide outputs via 12-bit DACs, according to jumper selections as follows:

0 to +5V
0 to +10V
±2.5V
±5V
±10V
4 to 20mA (source)

The current mode is operational for loop supplies of +12 to +40V. Both output channels are set to minimum scale at system initialization.

Output data is 12-bits, right justified in a 16-bit data field. The address space occupied by the output channels is in the same 2K byte area selected for input channels. Address lines ADR4/ to ADR9/ may be jumper selected anywhere in the 2K byte sector except at those addresses occupied by the input channels. The remaining address bits select the output channel and byte as shown in Table III.

Table III. Output Channel Addressing

Base + Address Bit 3/	2/	1/	0/	Channel
X	X	0	0	Ch1, Low Byte
X	X	0	1	Ch1, High Byte
X	X	1	0	Ch2, Low Byte
X	X	1	1	Ch2, High Byte

DC to DC Converter

The board contains a DC/DC converter to convert the +5V logic supply to the ±15V required by analog ciruitry.

Diagnostic Test

A diagnostic test program is included with BLC-8737 to allow testing and calibration of the analog circuits. Calibration is recommended when a full-scale range jumper is reset (input or output).

Channel Expansion

Sockets are provided to double the number of channels by inserting two multiplexers (LF 13508).

Specifications

Analog Input

Data Channels — 16 single-ended or 8 differential
Expandable to — 32 single-ended or 16 differential
Scan Mode — Sequential
Throughput Rate — 8500 conversions/second
Maximum Data Bandwidth — 200 Hz/ch (16 installed channels)
Full-scale Range —

0-10.24V		±10.24		0-20ma
0-5.12V	0-0.512V	±5.12	±0.512V	with user
0-2.56V	0-0.256V	±2.56V	±0.256V	installed
0-2.048V	0-0.2048V	±2.048V	±0.2048	250 ohm
0-1.024V	0-0.1024V	±1.024V	±0.1024V	resistors

Common Mode Voltage — +10.24V (signal plus common mode)
Overvoltage Protection — 125VAC
Programmable Gain
Software 1, 2, 5, 10
Jumper 1, 4, 10
Input Leakage Current — ⩽ 10nA @ 25°C (16 installed channels)
⩽ 60nA @ 0-55°C (16 installed channels)
Input Resistance — 3K ohms (power OFF)
⩾ 100M ohms (power ON)
Input Capacitance — ⩽ 100pF for ON channel (16 installed channels)
⩽ 10pF for OFF channel
Sample & Hold Feedthrough — ⩽ −80dB @ 200Hz
Crosstalk OFF to ON channel — ⩽ −80dB @ 200 Hz
Common-Mode Rejection ⩾ 60dB @ 200Hz (any gain)
ADC Resolution — 12 bits
Quantizing Error — ±½ LSB
Linearity Error — ⩽ ±½ LSB @ 55°V
⩽ ±1 LSB 0-55°C
Overall Accuracy — ⩽ ±0.05% FSR ± ½ LSB @25°C (Gain = 1)
⩽ ±0.07% FSR ± ½ LSB @25°C (Gain = 2, 5, 10)
Includes 3 sigma noise, linearity, offset and scale errors
No Missing Codes — 0-55°C

Analog Output

Data Channels — 2
Full-Scale Range — 0-5V and 0-10V @ 5mA
±2.5V, ±5V,
and ±10V @ ±5mA
4-20mA sourced (load may be grounded)
Current-Mode Supply Voltage — 12-40V (positive)
Max. Current-Mode Load Resistance (+24V supply) — 800 ohms
DAC Resolution — 12 bits
Linearity Error — (Voltage Mode) ⩽ ±½ LSB @ 25°C
⩽ ±1LSB 0-55°C

Overall Accuracy (Voltage or current mode)	⩽ ±0.05% FSR @25°C (includes linearity, noise, zero and scale errors)
Settling Time —	
Voltage Mode	⩽ 4μs to ±0.05% of FSR
Current Mode	⩽ 1ms to 0.05%
Monotonic	0–55°C

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE™ or open-collector TTL compatible. Fully BLC/SBC compatible.

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE™ or open-collector TTL compatible. Fully BLC/SBC compatible.
Connectors	
System Bus —	86-contact double-sided card-cage edge connector on 0.156" centers.
Analog —	One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 1–16. One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 17–32. One 26-contact double-sided card-edge connector on 0.1 inch centers for output channels.
Recommended Mating Connector (Analog)	50 contact double sided connector on 0.1 inch centers 3M 3415-001 AMP 2-86792-3 26 contact double-sided connector on 0.1 inch centers 3M 3462-0001 AMP 1-583715-1

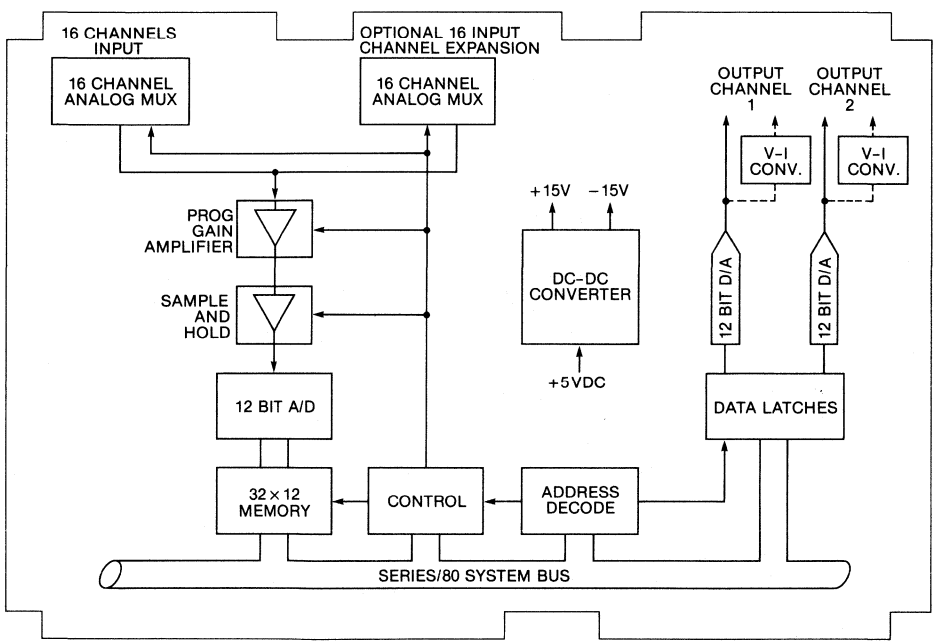
Power —	+5V ±5% @ 3A
Environmental —	
Temperature	0–55°C
Humidity	0–90% non-condensing
Physical —	
Height	6.75" (11.15 cm)
Width	12.00" (30.48 cm)
Depth	0.50" (1.27 cm)
Weight	18 oz. (510.3 g)

Order Information

BLC-8737-1 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, manual, and diagnostic test program in paper tape media.
BLC-8737-2 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, 2 analog voltage output channels, manual, and diagnostic test program in paper tape media.
BLC-8737-3 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, 2 analog voltage or current output channels, manual, and diagnostic test program in paper tape media.

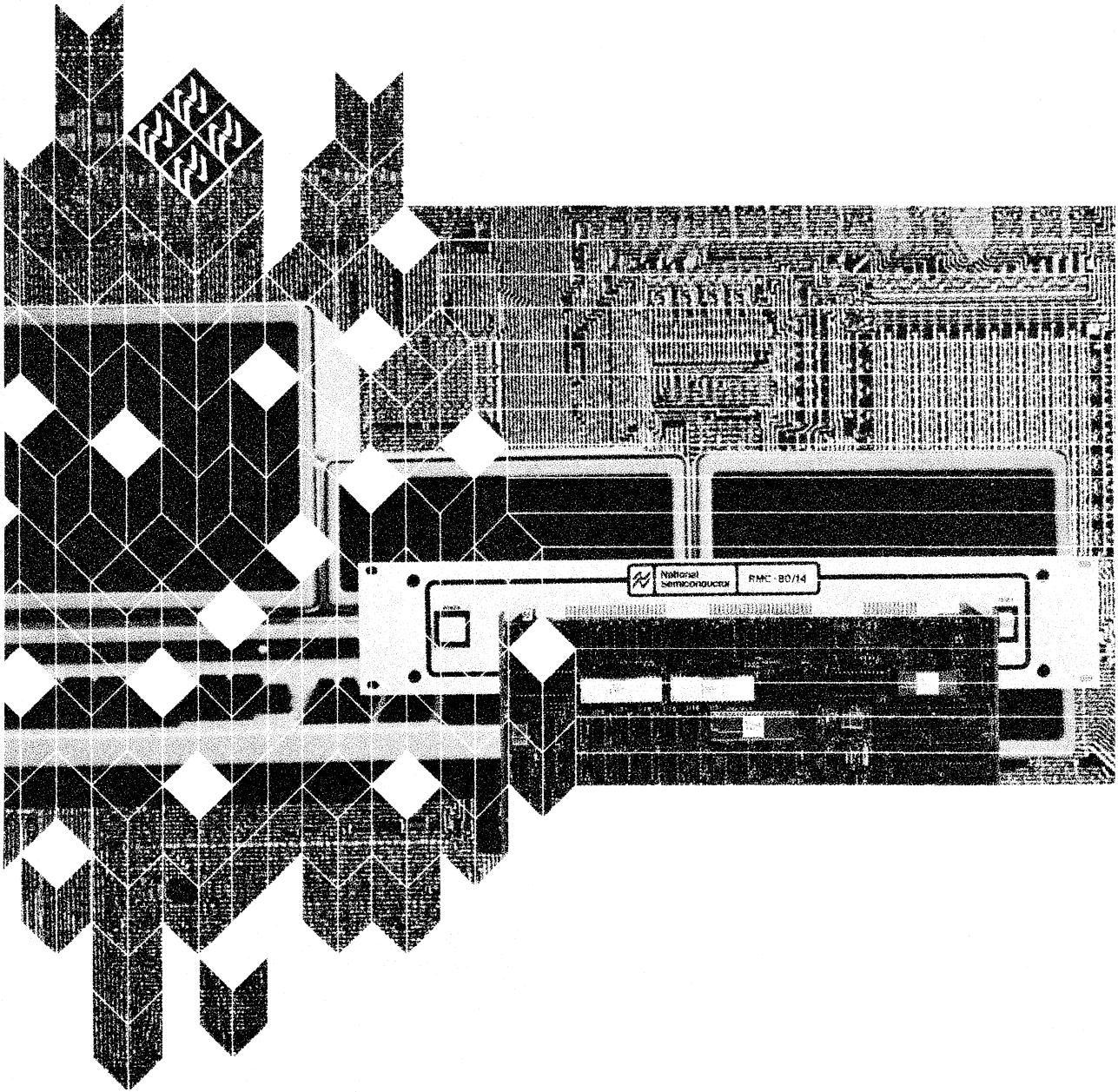
Documentation

420305890-001	BLC-8737 Analog I/O Board with Memory Hardware Reference Manual

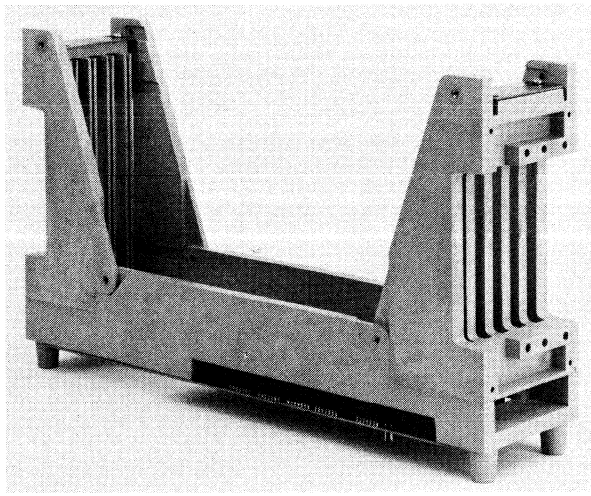


BLC-8737 DIAGRAM

Section 8
Card Cages and Power Supplies



BLC-604 and BLC-614 Card Cages



- **Series/80 System Flexibility**
  - 4 board incremental expansion capability
  - Requires only 3.5 inches of vertical space
- **Easy to Use — Includes:**
  - Backplane
  - Power supply connector
  - Threaded mounting holes

Product Overview

The BLC-604 and BLC-614 System Card Cages are ready-made, low-cost chassis for the housing and interconnection of National Semiconductor's Series/80 Board Level Computer products. Both the BLC-604 and BLC-614 Card Cages hold up to four Series/80 boards. The BLC-604 may be used in a stand alone configuration, while the BLC-614 is used as an addition to the BLC-604 when more space is required.

Functional Description

The BLC-604 is a 4-slot molded chassis including a backplane, with data, address and control signal bus, terminating networks, power supply connectors, and a bus extension circuit card edge connector. When more than one card cage is necessary a four slot BLC-614 expansion card cage is plugged into the bus expansion connector on the BLC-604. The BLC-614 contains an expansion connector for cascading additional BLC-614 card cages. The number of card cages to be cascaded is limited only by the bus drive capability or space limitations of the system. A BLC-604 or BLC-614 occupies only 3.5 vertical inches permitting highly compact packaging. The card cages can be conveniently mounted in any one of three planes.

Optionally available to support Series/80 systems are the 14 Amp BLC-635 Power Supply or 30 Amp BLC-665 Power Supply. Both power supplies include cables for connection to the BLC-604 and BLC-614. Also available is a power supply cable kit, the BLC-957, containing 2-foot cables for custom power supply connection to the card cage.

Specifications

Bus Connectors

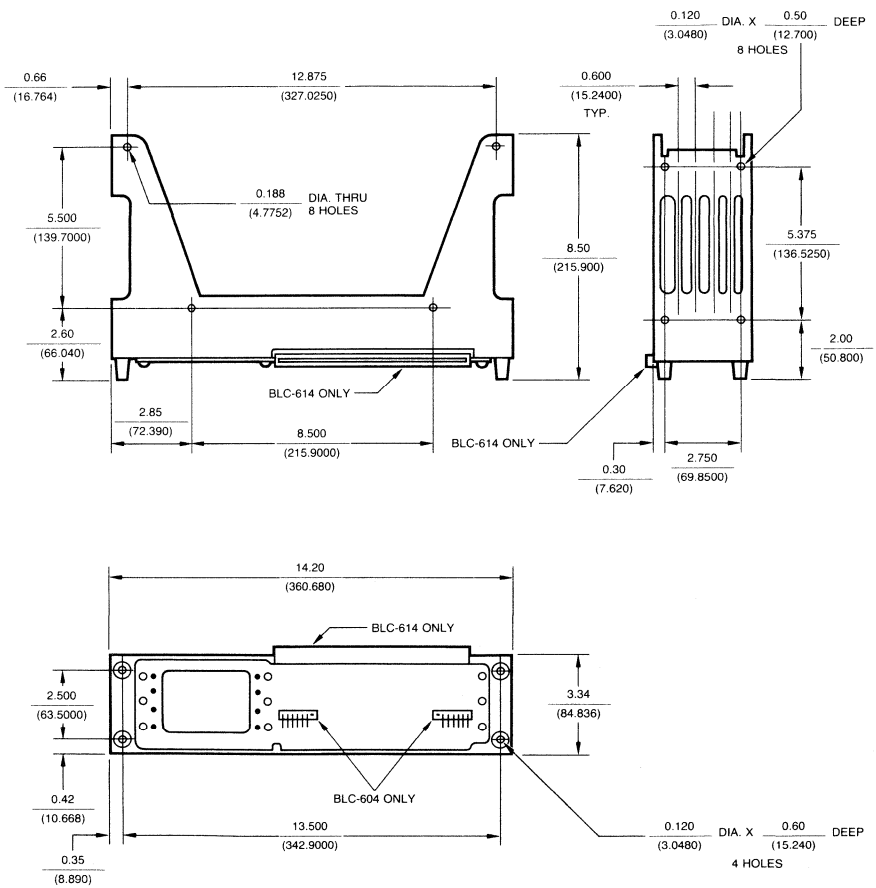
Signal	86 contact double-sided card cage edge connectors on 0.156 inch centers
Power	7-pin wafer with key (Molex crimp type 09-50-7071 or equivalent)

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —			
	Height	8.5 in.	(21.59 cm)
	Width	14.2 in.	(36.07 cm)
	Depth	3.34 in.	(8.48 cm)
	Weight	2.2 lbs.	(997.92 g)

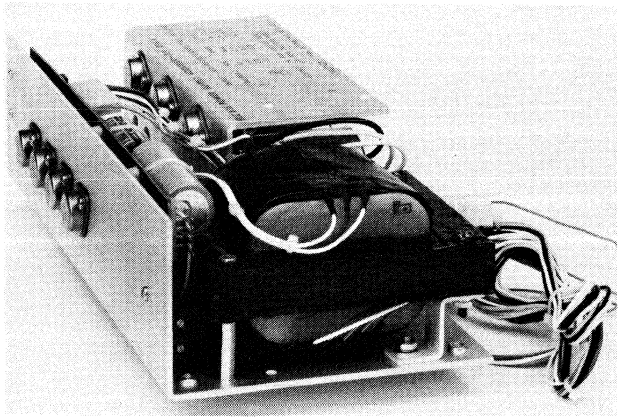
Order Information

BLC-604	Card Cage and Backplane Assembly
BLC-614	Expansion Card Cage Assembly
BLC-957	Power Supply Cable Kit

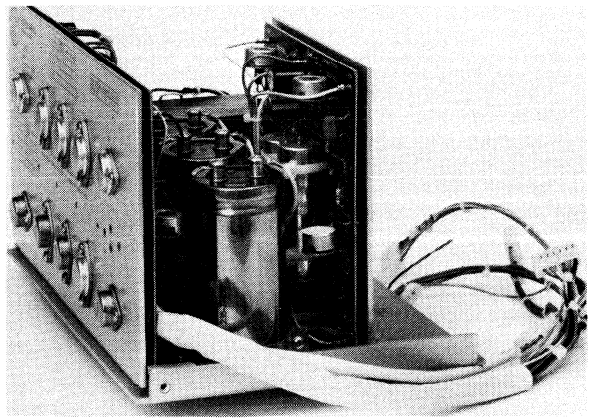


BLC-604 and BLC-614 Diagram

BLC-635 and BLC-665 Series/80 Power Supplies



BLC-635



BLC-665

- **Complete Power Supply Systems**
  - ±5, ±12 volt outputs
  - 110-115, 220-230 VAC input power
  - 47-63 Hz input frequency
- **High System Reliability**
  - AC low voltage sensing with TTL level output signal
  - Current limited outputs
  - Output overvoltage protection
- **Compatible with BLC/SBC Series/80 Systems**
  - BLC-635 supplies BLC/SBC CPU and three expansion boards
  - BLC-665 supplies BLC/SBC CPU and seven expansion boards
  - Mating cables for BLC/SBC-604 and 614 System Card Cages
  - BLC-635 — plug-replacement for SBC-635

Product Overview

The BLC-635 and BLC-665 are ready-made, low-cost power supplies for National Semiconductor's Series/80 Board Level Computers. These power supplies provide ±5 and ±12 volts of regulated DC power at maximum current over a temperature range of 0° to +55°C.

The BLC-635 provides power for a fully loaded BLC/SBC CPU with enough additional capacity to supply most configurations of three BLC/SBC memory, I/O, or other expansion boards.

The BLC-665 supplies approximately twice the rated power of the BLC-635. The BLC-665 will power a fully loaded BLC/SBC CPU board and most combinations of seven additional expansion boards.

All outputs are current limited and have overvoltage protection. The AC input is fused for either 100-115 VAC or 200-230 VAC operation.

DC power is carried on cables keyed for compatibility to the BLC-604 System Card Cage. The BLC-635 and BLC-665 utilize circuitry to sense an AC power failure or low line conditions and will generate a TTL compatible signal for orderly system shutdown.

Functional Description

Output Current Rating

VDC	BLC-635	BLC-665
+5	14 A	30 A
−5	0.9 A	1.75 A
+12	2.0 A	4.5 A
−12	0.8 A	1.75 A

Current limit approximately 20% above rated values.

Output Adjust Range

±5% minimum on all outputs around nominal voltage

Line Regulation

±0.1% on all outputs for 10% line change

Load Regulation

±0.1% on all outputs for 50% load change

Output Ripple and Noise

10 mv peak-to-peak maximum on all outputs from DC to 500 KHz

Stability

±0.05% on all outputs for 8 hours at constant line, load, and temperature after 30 minutes of warm-up

Transient Response

±5% on all outputs maximum for less than 50 microseconds with 50% load change

Remote Sensing

Provided at P8 connector for +5 volts

Chassis Ground Insulation

All output returns isolated from chassis ground

Overvoltage Protection

Provided on all outputs and factory set to trip within the following ranges:

Output Voltage	OVP Trip Range
+5V	5.8V to 6.6V
−5V	−5.8V to −6.6V
+12V	14V to 16V
−12V	−14V to −16V

Overload and Short Circuit Protection

+5V — Foldback current limiting with automatic recovery

−5V, +12V, −12V — Current limited to extent no damage will occur for extended overload condition

---

Specifications

Input Power — 100, 115, 215, 230 VAC ± 10%
47-63 Hz

Input Fusing — 100/115 VAC 3.0 A slow blow
200/230 VAC 1.5 A slow blow

Connectors —

	BLC-635/665 Connectors			Recommended Mating Parts		
		Part Number			Part Number	
	Type	Molex	Amp	Type	Molex	Amp
AC Input (P2)	Connector Pin	03-09-2052 02-09-2118	N/A	Connector Pin	08-09-1052 02-09-1118	N/A
DC Output (P6, P8)	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2	Right Angle Connector Assembly	09-66-1071	87194-6
"AC Low" Detection (J3)	Connector Assembly	09-67-1072 or 09-66-1071	87262-7	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

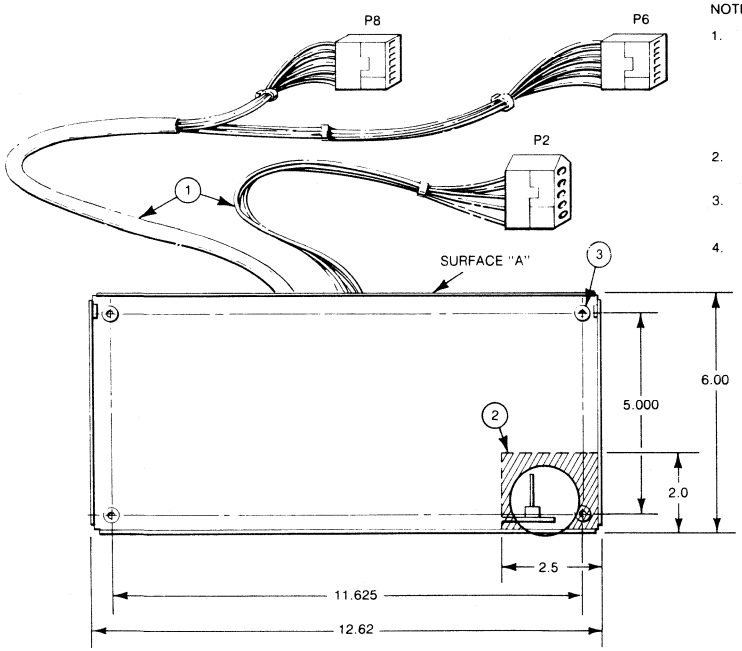
	BLC-635	BLC-665
Height	3.19 in. (8.1 cm)	6.62 in. (16.8 cm)
Width	6.03 in. (15.3 cm)	6.50 in. (16.5 cm)
Depth	12.65 in. (32.1 cm)	12.65 in. (32.1 cm)
Weight	13 lb. (5.9 kg)	21 lb. (9.6 kg)

Order Information

BLC-635	14 A Power Supply, includes cables for connection to card cage.
BLC-665	30 A Power Supply, includes cables for connection to card cage.

Documentation

420305489-001	BLC-635 Power Supply User's Manual
420305220-001	BLC-665 Power Supply User's Manual

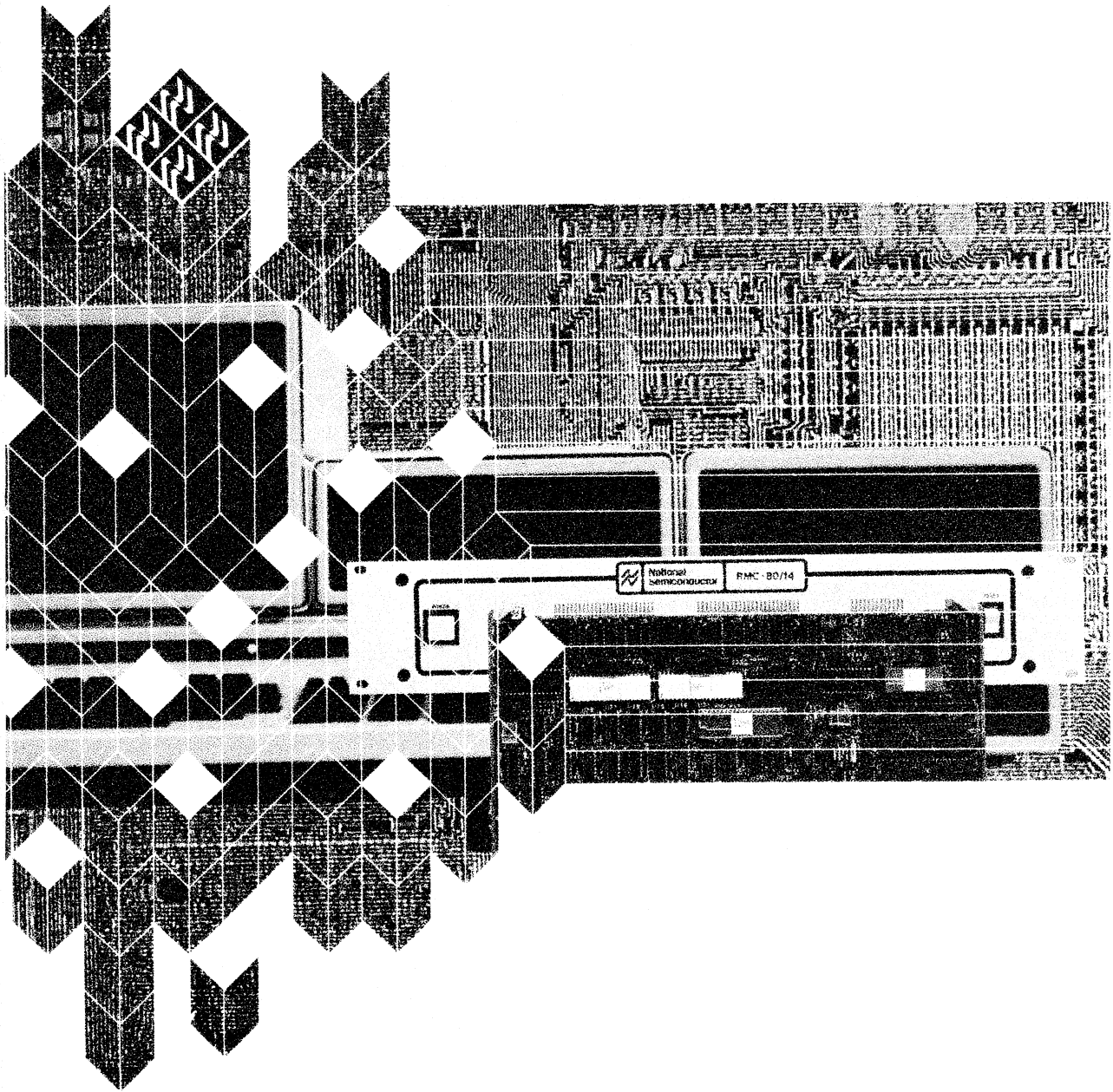


NOTES:

1. Harness lengths are from center of surface "A" to connector
   a. DC OUTPUT 24 inches to P6 conn.
   b. DC OUTPUT 16 inches to P8 conn.
   c. AC INPUT 12 inches to P2 conn.
2. Location of "AC LOW" signal connector is within cross hatched volume, orientation may vary.
3. All four mounting holes threaded for 8-32 machine screws.
4. BLC-665 has 2 each connectors P6, P8 to enable connection to two card cages.

BLC-635 Diagram

Section 9
Development System



STARPLEX™ Development System

- **A Total Development System**
  - Hardware:
    CPU, Floppy Discs, Video Monitor, Keyboard
  - Software:
    Disc Operating System, Debugger, Editor, Macro Assembler, FORTRAN, BASIC, On-Board ROM Diagnostic and Utilities
  - Options:
    Emulators, PROM programmer, Printers, STARLINK, Cross Assemblers
- **Easy to Use**
  - Function keys direct system
  - Prompting menus guide operator entries
  - Comprehensible error messages
  - Keystroke-driven editor
- **Full Product Line Support**
  - Supports 8080, 8048, 8049, 8050, NSC800, 8085, 8070 and Z-80-based microprocessor systems
  - Expandable with industry standard BLC/SBC boards

Product Overview

The STARPLEX™ Development System is a general purpose microcomputer and microprocessor development system. New levels of operating simplicity have been designed into the STARPLEX system to significantly reduce the amount of time spent on product development. By getting the user into actual application work sooner and with fewer mistakes, the STARPLEX system allows the user to take full advantage of time spent at the console.

A Total System

The STARPLEX design combines all the components required for the entire development task in one complete system. The STARPLEX package includes an 8080-based CPU board, 64K bytes of RAM, 1M byte of disc storage, a video monitor and keyboard. The standard STARPLEX software package includes a disc operating system, assembler, debugger, editor, linker, loader, FORTRAN, BASIC, on-board ROM diagnostic and utilities. Options available are: an in-system emulator for real-time debugging of customized hardware and software, PROM programmer personality modules for programming, verifying and copying PROMs, STARLINK™ for transferring files between STARPLEX™ and MDS Development System, and cross assemblers.

Easy to Use

The STARPLEX System reduces the time a user must spend at a terminal by making many complex functions accessible through one easy keystroke. System commands are initiated by clearly marked function keys which invoke prompting menus to guide the user through each task. These function keys eliminate the need to memorize system commands and various command options. As a result, there is no need to refer to lengthy documentation, and errors or delays caused by incorrectly entered commands are eliminated.

Recognizing that a great deal of the user's time is spent on creating and changing source code, the designers of the STARPLEX system have devoted special attention to the text editing facility.

A set of special function keys directs the STARPLEX editor, allowing corrections to be made with single keystrokes. Also, the powerful "string mode" commands allow search and replacement of character strings as well as block moves. An entire file may be quickly and easily reviewed or altered. The number of mistakes is reduced because the data and changes are immediately displayed. Backup files are automatically created, protecting the user from accidental loss of data. Because the STARPLEX system is easy to use, learning time is considerably shortened. A first time user can be productive within a half hour. Also, as users make more efficient use of the system, machine availability is maximized.

Full Product Line Support

When a user buys a STARPLEX System he can be assured it will meet both today's and tomorrow's development needs. All the boards within the STARPLEX System are members of National's Series/80 family and use the standard Series/80 bus, making the system expandable with the more than 40 boards presently available in this series.

The STARPLEX System supports development for the 8080A, 8048, 8049, 8050, NSC800, 8070, Z80 and 8085 processors and will support all future National and other popular microcomputer and microprocessor products.

The Result — Cost Effectiveness

The most important feature of the STARPLEX System is that it saves development time. Its ease of use allows the designer to concentrate on solving the application problem, rather than learning how to operate the system. With the STARPLEX system, the effectiveness of a company's most valuable resource — "engineering manpower" — is maximized.

Functional Description

Hardware Modules

STARPLEX components are packaged into modules which form a unified system when placed together. The modules are durable, with housings constructed of 1/8 inch aluminum and front panels of molded lexan foam.

STARPLEX is designed for easy maintanance. Snap-down doors on the base module make it easy to access the card cages and circuit boards. Interconnecting cables between all modules and boards are routed to the rear of the system and covered by easily removable cable channels. Thus, cables are out of sight and protected from accidental damage. All cables, including the single AC power distribution system, are plug detachable at both ends, making it easy to disconnect modules and reconfigure the system.

Human engineering concepts have directed the design of each STARPLEX module to make the man-machine interface as natural as possible. For example, the video monitor screen has antireflective coating to minimize glare, and light-emitting diodes in certain keys provide operator awareness of their selection. Even cooling fans have been located to minimize noise levels.

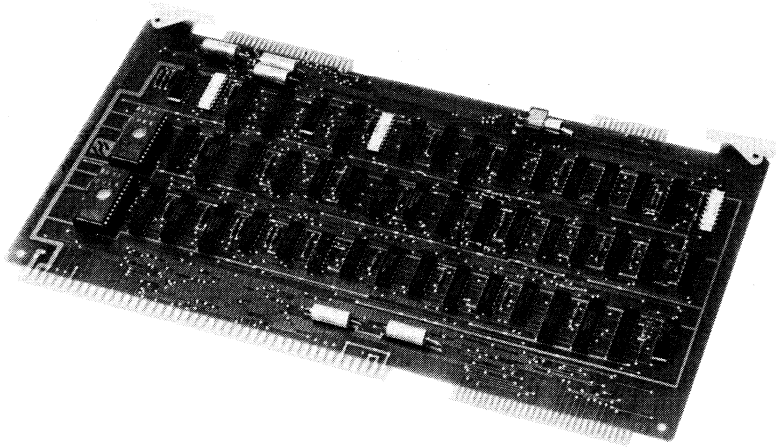
STARPLEX Electronics

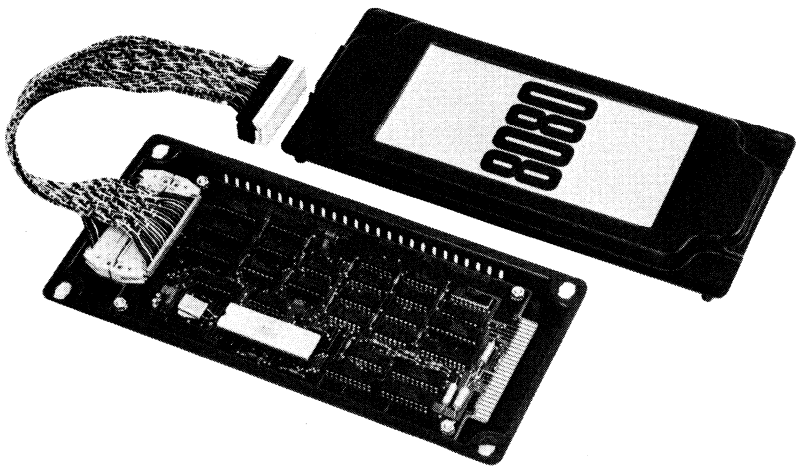
Four Series/80 boards make up the STARPLEX electronics: the main CPU board (based on the BLC-80/204), the video monitor/keyboard controller (BLC-8229), the floppy disc controller (BLC-8222) and a 64K memory board (BLC-064).

These boards communicate with each other via the standard BLC system bus. The CPU, BLC-8229 and BLC-8222 all have multi-master bus logic on their respective boards allowing them to share the system bus. The BLC-8229 and BLC-8222 communicate with the CPU using Direct Memory Access and programmed I/O.

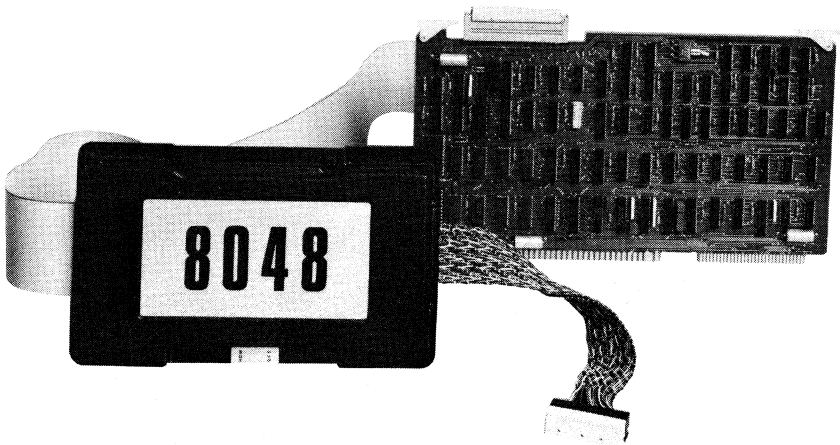
The optional printers and PROM programmer personality modules communicate with the CPU through two programmable parallel I/O ports. An RS232C port on the CPU is available and permits both asynchronous and synchronous communications for use with a printer or a communications link such as STARLINK.

Individual circuit boards are built to National's high manufacturing quality standards, utilizing techniques such as computer aided layout and auto insertion. All boards and the system as a whole are tested dynamically under system load conditions at elevated temperatures as part of a thorough factory burn-in.

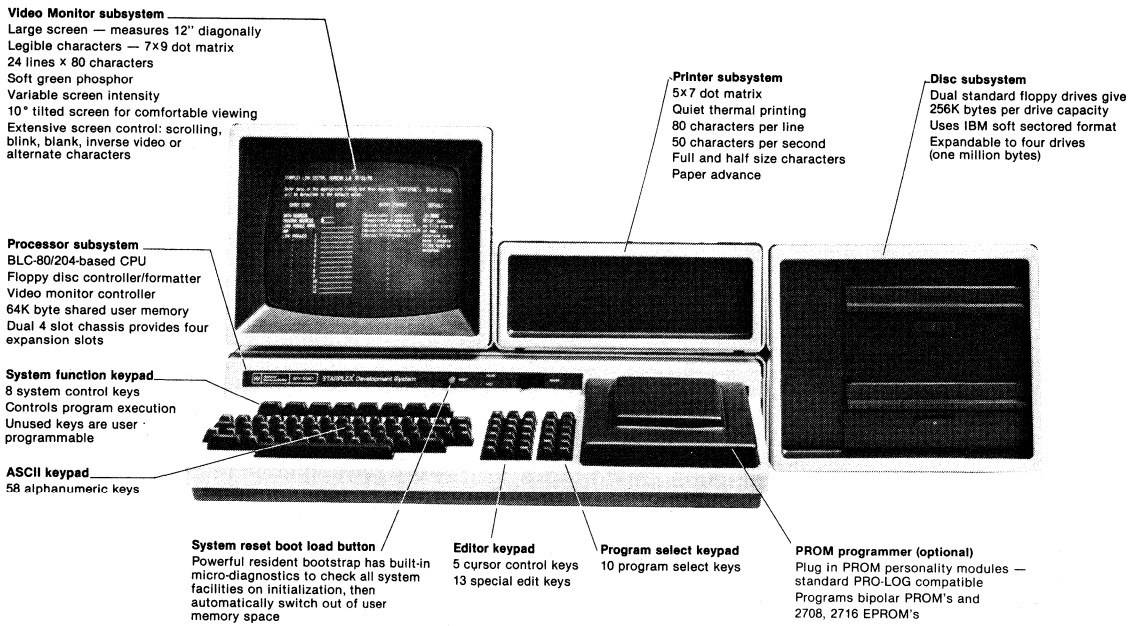


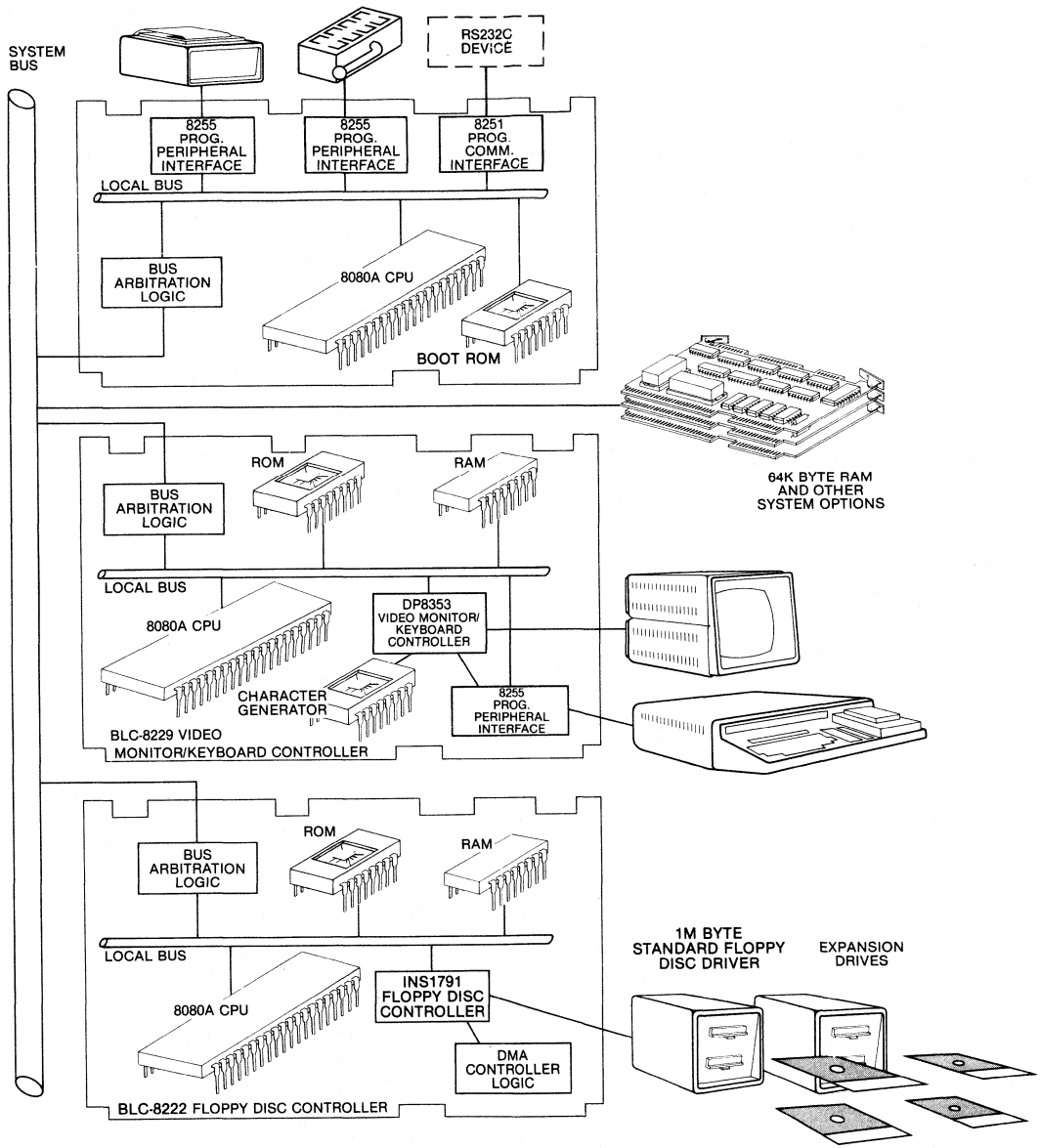


8080 ISE


8048

8048 ISE


Video Monitor subsystem
Large screen — measures 12" diagonally
Legible characters — 7x9 dot matrix
24 lines x 80 characters
Soft green phosphor
Variable screen intensity
10° tilted screen for comfortable viewing
Extensive screen control: scrolling, blink, blank, inverse video or alternate characters
Printer subsystem
5x7 dot matrix
Quiet thermal printing
80 characters per line
50 characters per second
Full and half size characters
Paper advance
Disc subsystem
Dual standard floppy drives give 256K bytes per drive capacity
Uses IBM soft sectored format
Expandable to four drives (one million bytes)
Processor subsystem
BLC-80/204-based CPU
Floppy disc controller/formatter
Video monitor controller
64K byte shared user memory
Dual 4 slot chassis provides four expansion slots
System function keypad
8 system control keys
Controls program execution
Unused keys are user programmable
ASCII keypad
58 alphanumeric keys
System reset boot load button
Powerful resident bootstrap has built-in micro-diagnostics to check all system facilities on initialization, then automatically switch out of user memory space
Editor keypad
5 cursor control keys
13 special edit keys
Program select keypad
10 program select keys
PROM programmer (optional)
Plug in PROM personality modules — standard PRO-LOG compatible
Programs bipolar PROM's and 2708, 2716 EPROM's



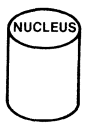
STARPLEX Multiprocessor System Diagram

Software

STARPLEX software is completely thought out from a functional standpoint, carefully engineered to be easy to understand and use and thoroughly integrated into the total system. Every aspect is designed to assist the user in rapidly developing microprocessor-based systems from the ground up.

The elegance of STARPLEX software lies in its ability to make the complicated process of program development appear simple to the user.

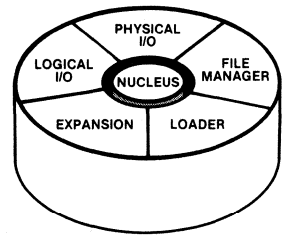
The software system is structured as a series of rings around a nucleus. Segments of these rings can be changed or added for future development requirements such as other high-level languages, file handlers or special user-defined routines.



NUCLEUS

The nucleus of the STARPLEX operating system controls and allocates system resources for the higher level processes.

- Provides synchronization and communication facilities for higher level asynchronous processes
- Services all hardware interrupts
- Provides interval timer functions
- Completely device-independent



LEVEL I

Level I of the operating system provides system housekeeping functions and coordinates access to system resources. It includes a file manager, an I/O control system and a loader.

File Manager

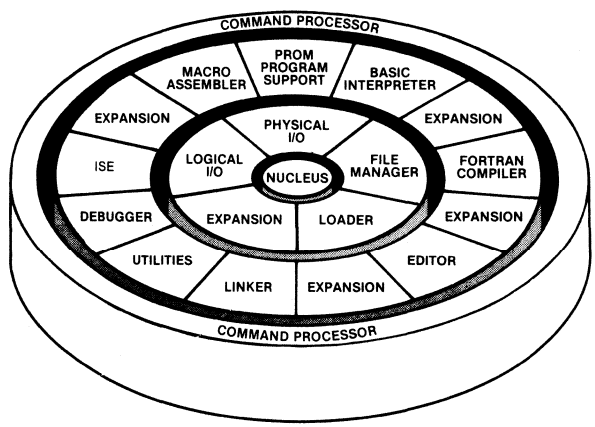
The file manager organizes, stores and retrieves data and programs stored on the diskette.

- Maintains a directory
- Allows multiple file attributes
- Uses a "hierarchical linked list" structure
- Supports random access

I/O Control System

The I/O control system is designed to eliminate the need for the user to understand the physical I/O characteristics of each individual device and presents a simplified, logical device-independent architecture.

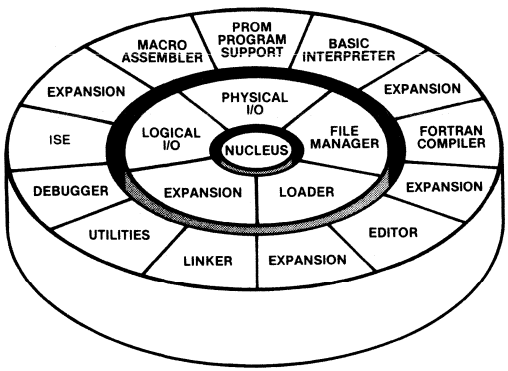
- Provides overlapped I/O commands
- Allows files to be accessed by name
- Handles error conditions



Loader

The loader brings programs into main memory at specified locations.

- Provides "load and go" mode
- Allows controlled load mode — starting address returned to calling program



LEVEL 2

Level 2 of the operating system provides the "development services" including a linker, a CRT-oriented editor, utilities, a debugger, PROM programmer support, Macro assemblers, BASIC and FORTRAN IV.

Linker

The linker combines selected relocatable object modules created by the assembler or language compiler into an executable run time module.

- Assigns absolute addresses to load modules
- Produces a memory map of linked components
- Searches system and user libraries for unresolved external references

Editor

The STARPLEX editor is an easy-to-use CRT -oriented text editor.

- Function key driven
- String search and replace
- Forward and backward paging
- Block moves
- Automatic source file backup
- Traps illegal commands

Utilities

General utilities provide routine maintenance functions.

- Transfer data files between devices
- Obtain diskette directory listings
- Format diskettes
- Modify file attributes
- Rename files

Debugger

The program debugger simplifies 8080 program checkout by allowing program execution to be monitored and altered.

- Allows single step control
- Permits eight breakpoint assignments
- Displays program counter and registers at breakpoints
- Memory references are absolute or relative to one of the relocation registers

PROM Programmer Support

The PROM programmer support software manages the optional PROM personality module functions.

- Allows PROM code to be listed, verified and copied
- Data stored in a PROM can be transferred to or from another PROM, a diskette file, memory, the video monitor or keyboard.

Macro Assemblers

The Macro assemblers assemble 8080, 8085, 8048, 8070, NSC800, and Z80 mnemonic code and allow operator definition of useful higher level instructions called "Macros" which are then expanded into a sequence of machine level instructions.

- Generates absolute or relocatable object modules
- Conditional assembly parameters
- Allows external references

FORTRAN IV

The FORTRAN IV compiler on the STARPLEX system meets the ANSI X3.9-1966 standard and includes the following enhancements:

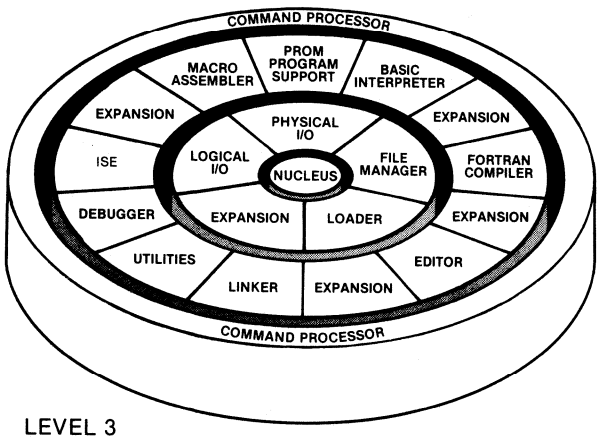
- PEEK and POKE — allow direct access to memory
- INP and OUT — allow direct I/O access

- Comprehensive subroutine library
- Supports user-written I/O drivers
- Random access disc I/O
- Allows assembly language subroutine calls

BASIC

The STARPLEX BASIC compiler/interpreter conforms to the Dartmouth defined BASIC with extensions:

- PEEK and POKE — allow direct access to memory
- INP and OUT — allow direct I/O access for non-STARPLEX devices
- Complete string operators
- Multi-dimensional arrays
- Extensive debugging and programming aids — trace, edit, direct mode, renumber



LEVEL 3

The Command Interpreter is the interface between the operating system and the human operator.

- Function key driven
- Verifies user requests
- Provides menus and prompting for system commands

Specifications

Memory — 64K bytes

Floppy Disc —

Format	IBM compatible, soft-sectored
Capacity	512K bytes per drive
Maximum Capacity	1 million bytes (4 drives)

Printers —

Type	Thermal
Speed	50 characters per second
Width	80 columns
Character Type	5x7 dot matrix
Type	Impact
Speed	120 characters per second
Width	132 columns
Character Type	7 x 9 dot matrix

Video Monitor —

Matrix	7x9 dot
Display Array	80 columns by 24 lines
Phosphor	P2 green

Power — 115VAC, 60Hz, 10 amps (max) or 230VAC, 50Hz, 5 amps (max)

Base Module	644 Watts
Floppy Disc Module	966 Watts
Thermal Printer	126 Watts
Impact Printer	360 Watts
Video Monitor	34 Watts

Physical —

	Base Module	Floppy Disc Module	Thermal Printer	Impact Printer	Video Monitor
Height	5.75 in. 14.6 cm	11.5 in. 29.2 cm	5.75 in. 14.6 cm	8 in. 20.3 cm	11.5 in. 29.2 cm
Width	26 in. 66 cm	13 in. 33 cm	13 in. 33 cm	24.5 in. 62.2 cm	13 in. 33 cm
Depth	26 in. 66 cm	19 in. 48.3 cm	19 in. 48.3 cm	18 in. 45.7 cm	19 in. 48.3 cm
Weight	68 lb. 30.8 kg	50 lb. 22.7 kg	28 lb. 12.7 kg	60 lb. 27 kg	29 lb. 13.2 kg

Order Information

SPX-80/40	STARPLEX Development System with Thermal Printer (60 Hz)
SPX-80/41	STARPLEX Development System without Printer (60 Hz)
SPX-80/42	STARPLEX Development System with Impact Printer (60 Hz)
SPX-80/51	STARPLEX Development System with 1 Megabyte Disc Storage (60 Hz)
SPX-80/61	STARPLEX Development System with 2 Megabyte Disc Storage (60 Hz)

Note: To order 50 Hz add the letter "E" to the order number.

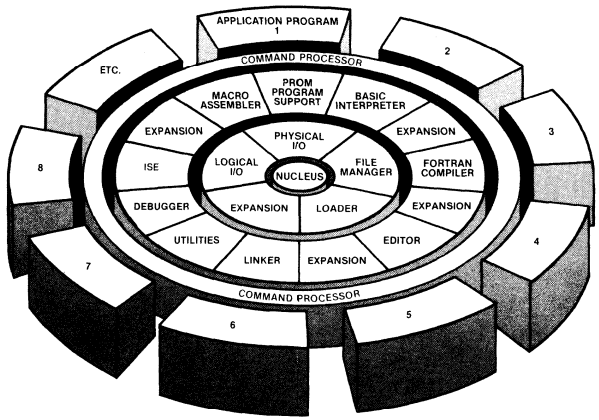
Options

SPM-A02	PROM programming interface plus software
SPM-A02-1	PROM programming module for programming 2708 EPROMs
SPM-A02-2	PROM programming module for programming 2716 EPROMs
SPM-A06-1	STARPLEX 1 Megabyte Dual Disc Expansion
SPM-A06-2	STARPLEX 2 Megabyte Dual Disc Expansion
SPM-A08	In-System Emulator Module
SPM-A09-1	8080 Emulator Package
SPM-A09-2	8048 Emulator Package
SPM-A09-3	8070 Emulator Package
SPM-A10	Z-80 Development Package
SPM-A50	Thermal Printer
SPM-A55	Impact Printer
SFW-A001-1C	8048 Cross Assembler
SFW-A002-1C	8070 Cross Assembler
SFW-A003-1C	NSC800 Cross Assembler
AEE-A001	STARLINK — SPX/MDS220, 230 Link
AEE-A002	STARLINK — SPX/MDS800, 888 Link

Documentation

420305546-001	STARPLEX System Reference Manual
420305788-001	STARPLEX System Software Reference Manual
420305789-001	STARPLEX Macro Assembler Software User's Manual
420305790-001	STARPLEX FORTRAN Compiler Software User's Manual
420305791-001	STARPLEX BASIC Interpreter Software User's Manual
420305586-001	BLC-8201/8221 Floppy Disc Controller Hardware Reference Manual
420305804-001	BLC-8222 Double Density Floppy Disc Controller Hardware Reference Manual
420305587-001	BLC-8228/8229 Video Monitor/Keyboard Controller Hardware Reference Manual
420305793-001	STARPLEX Hardware Maintenance Manual
420305521-001	BLC-80/204 Board Level Computer Hardware Reference Manual
420305529-001	BLC-032/048/064 32/48/64K RAM Board Hardware Reference Manual
420305869-001	In-System Emulator Reference Manual
420305653-001	SPM-A09-1 8080 ISE Target Board User's Manual
420306065-001	SPM-A09-2 8048 ISE Target Board User's Manual
420306155-001	SPM-A10 ZSTAR™ Z-80 Development System Reference Manual
420306154-001	Z80 Assembler Manual
420306064-001	8048 Family Cross Assembler User's Manual

STARPLEX™ Disc Operating System



- **Complete Self-Contained System**
  - Full support of all hardware
  - Complete array of software tools
- **Simplified Program and User Access to All Peripherals**
  - Device-independent I/O
  - Dynamic logical unit assignment
  - Names files and devices
- **Convenient Control Facilities**
  - Special function keypads
  - Single keystroke command functions
- **User-Oriented Support Programs**
  - Editor controlled by special function keys
  - High level languages for rapid application program development
  - English language error messages
- **Full Set of Utilities**
  - Linker — allows modular program construction
  - Loader — locates programs on disc and loads them into memory
  - Debugger — minimizes program checkout time

Product Overview

Yesterday's development systems were designed with only one aspect of the development function in mind — the hardware. Today people, not hardware, are the most costly element of the development process, and development systems now must maximize the utility of the human resource.

The STARPLEX Disc Operating System (DOS) is a general purpose, user-oriented software system designed to eliminate tedious time-consuming tasks normally associated with program preparation, debugging and maintenance. All software required to develop, debug and maintain user applications in Assembler Language, FORTRAN IV, and BASIC is provided with the STARPLEX System. The software includes: an Editor for creating/editing source files; high level languages for easy program implementation; Macro Assemblers for generating absolute/relocatable object modules; an I/O management system for accessing and controlling peripheral devices; a Linker for gathering all program modules into a run file; a PROM programmer support package and In-System Emulation support packages for run time program testing.

One of the key design features of the STARPLEX DOS is its ease of use. The special function keypads make access to the operating system,

languages and system utilities as easy as a single keystroke. With STARPLEX DOS it is not necessary to wade through lengthy instruction manuals in order to perform a simple operation; instead, the clearly labeled function keys perform complex and repetitive functions without requiring the operator to memorize awkward command structures.

Specially designed screen menus augment the special function keys. Press a key and a menu of commands appears on the CRT screen. This menu has fill-in-the-blank fields that define the information needed from the operator in order to perform the function. By using the TAB key the user selects the function and fills in the necessary information. Pressing the RETURN key signals the system to take action. The standard system menus may be modified to suit individual needs or entirely new menus created to fit the application problem.

The extensive and easy-to-use system and program control features, utility functions and data management facilities free the user to concentrate on problem-solving rather than system management.

Functional Description

The STARPLEX Disc Operating System is structured as a series of layers, each inner layer providing program services to the outer layers.

The nucleus forms the central core of the system. Its primary function is to provide synchronization and communication facilities for higher level processes. This is accomplished by a set of queues and associated operations used to implement a message passing structure for communication to and from the outer layers. In this manner the nucleus controls and allocates system resources for the higher level processes.

The first layer around the nucleus provides system housekeeping functions and consists of a file manager, input/output control system and a program loader. This layer coordinates access to system resources and relieves higher level functions of the need to specify the particular characteristics of the various input and output resources.

The next layer provides utilities and interface to higher level languages. Finally, the command processor at the outer edge is the interface between the operating system and the human operator. It responds to keyboard commands, checks their validity and invokes the appropriate system service requests.

System Function Keys

In order to simplify user control and access, several special function keypads have been provided. These keypads allow the user to call complex or time-critical functions with a single keystroke. Keys are provided to PAUSE and CONTINUE system activity, END or ABORT programs, invoke the EDITOR, FORTRAN compiler, Macro Assemblers, Linker, In-System Emulators, BASIC interpreter and other utility programs, and request HELP from the system. When appropriate, the command processor will ask for supplementary information such as file name or for confirmation of the command.

I/O Control System

The input/output control system is designed to relieve the user of the need to understand the physical I/O characteristics of each individual device, and is implemented at two levels. At one level the program interface is to a logical input/output device, allowing a program to be device-independent. This method permits the user to redirect output of a program to any available device at run time without having to re-compile or re-assemble the program. This often results in significant time savings in the program debug phase. The second level is the physical device driver interface. At this level the logical I/O service routine communicates with the device driver and translates the logical I/O request to device characteristics. Direct calls to the device driver also allow the user full access to individual device characteristics for special applications problems.

The I/O processor provides several I/O calls at the system level to maximize the flexibility of the system. READ and WRITE calls transfer data between the specified device and main system memory. Control is returned to the calling program after completion of the I/O transfer. To provide greater system design flexibility two additional I/O calls (READ INITIATE and WRITE INITIATE) are provided that allow overlapped I/O. READI and WRITI calls initiate I/O processing but return control to the calling program without waiting for the I/O process to be completed. The calling program can later check for an I/O-complete status using an IOCHK call or place itself in a "wait for completion" state with IOWAIT.

Set keyboard mask (KBDMSK) is another facility that adds significant flexibility to system design. This service allows the calling program to specify which keys the system should accept and which keys should be responded to with an error tone. KBDMSK allows the program to dynamically change the keyboard environment according to the

current program mode needed. The STARPLEX editor uses this facility extensively to control inputs to the various editing modes. This capability may also be used to specify that the program itself wishes to control and respond to system functions such as CANCEL, END, CONTINUE, and HELP.

File Management

File Structure:

Files in STARPLEX are identified by a three part file descriptor consisting of volume name, file name, and extension. An example of a file descriptor is FDSn:PROG.FOR, which specifies a disc known to the system as "FDSn" and a FORTRAN source file named PROG.

The indexed file structure allows the manipulation of logical records that are automatically blocked and deblocked. These logical records can be accessed one after the other by sequential I/O calls or randomly by specifying a logical record number. The indexed file is open-ended, does not require pre-allocation of disc space, and allows new data to be appended to it. Files may be allocated, named, deleted, renamed or protected by operator command or program control. This capability enables programs to dynamically change the operating environment and results in greater flexibility.

File Protection:

Three types of protection attributes are available. Files may be designated as write protected so that no program may write over the stored data. A transparent mode designates permanent or semi-permanent files that are not listed when the DIRECTORY LIST command is executed, unless specifically requested. This significantly shortens the list the operator normally reviews in the program development process. The third protection attribute specifies a permanent mode. Files designated as permanent may not be deleted.

Editor

The STARPLEX System Editor is a powerful system tool for the creation and maintenance of source code. The Editor may be used to generate and modify source text for any programming language as well as data files and screen formats.

A special Editor keypad is provided that reduces most Editor command functions to a single keystroke. Using this keypad the operator can insert or delete characters or lines, scroll through the text file forward or backward a line or a page at a time, position the cursor and set tabs simply by pressing a key. The "STRING MODE" key allows the user to enter powerful string commands such as FIND, REPLACE, INSERT, DELETE, and ADD AND STORE for block moves.

Linker

The Linker combines selected relocatable object modules created by the assembler or language compiler into an executable run time module. System libraries and user-specified libraries are searched to satisfy any unresolved external references. A comprehensive load map may be generated which lists resolved and unresolved external references with their memory locations.

It is possible to specify that sections of a program be loaded into absolute or relative segments of memory. This allows separation of data and program code when linking programs for RAM destinations or when creating a module for the programming of PROM's.

Loader

The loader brings programs and data into main memory at specified memory locations. If the object file is relocatable it loads the file and performs the translation from relocatable to absolute format. After loading, the loader provides for direct execution (load and go) or controlled execution (load only) by the calling program.

Macro Assemblers

The Macro Assemblers generate absolute or relocatable object modules from instruction statements and directives. Listings may be generated which include original source statements, machine code with memory address (absolute or relocatable), and a list of referenced symbols. External statements are provided to permit separately generated modules to reference one another and have addresses resolved at link time. Conditional assembly directives direct the assembler to assemble or ignore certain sections of code. Macros simplify generation of repetitive code and standard subroutines and provide the vehicle for standardizing system calls.

Debugger

The system debugger monitors and alters the execution of 8080 programs in STARPLEX memory. Memory references are absolute or relative to one of the eight relocation registers. The program counter, accumulator, memory and all hardware register contents may be inspected and changed. Programs may be executed at full speed or flow traced by using the single step function. Multiple breakpoint capability is provided with automatic content save and restore. When used, breakpoints transfer control to the debugger as they are

encountered during program execution and are automatically restored after breakpoint execution.

General Utilities

Utility programs provide file maintenance capabilities such as copy, rename, delete and protect. The transfer of information between devices is handled by the "copy" function. For example, to display a file simply "copy" the file to the video monitor. A complete roster of files may be obtained which lists the names, protection attributes and length of all files contained on the diskette. The system also provides facilities to format and backup diskettes.

"Wild card" commands are available for all file maintenance utilities. This allows the user to perform several functions with a single command. For example, to delete all files with an extension of BIN, the user would type "DELETE *. BIN.".

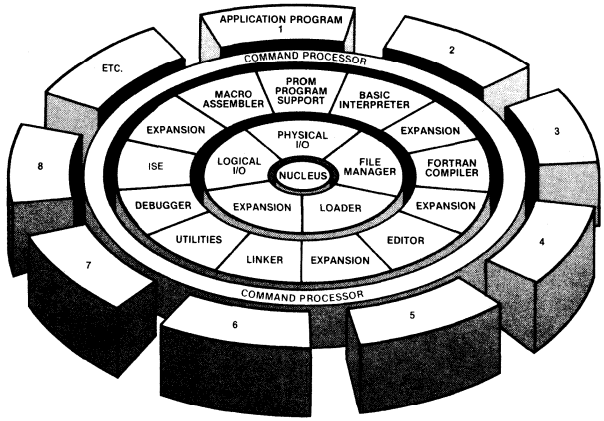
System Calls

OPEN	Prepare file for access.
CLOSE	Update pointers and make file unavailable for access.
READ	Transfer a block or line of data from specified file to host memory and wait for completion.
READI	Begin to transfer a block or line of data from specified file to host memory and return control to caller.
WRITE	Transfer a block of data from host memory to specified file and wait for completion.
WRITEI	Begin to transfer a block of data from host memory to specified file and return control to caller.
DELETE	Remove file entry from directory and release file storage.
FPOS	Set or determine current position of a file pointer.
IOCHK	Check for completion of previous READI or WRITEI command.
IOWAIT	Wait for completion of previous READI, FPOS, or WRITE I command.
ATTRIB	Set or reset attributes of an opened file.
RENAME	Change name of a file in file directory.
DISKIO	Direct access to diskette without file management control.
EXIT	Normal return to operating system.
EREXIT	Abnormal return to operating system.
KBDMSK	Masks the availability of keyboard characters to a program.
INFO	Sets time, date and default system devices
IOINFO	Returns information about currently open file
DELAY	Halts execution of user program for specified time interval

Order Information

STARPLEX™ Disc Operating System is included with the STARPLEX Development System.

STARPLEX™ BASIC



- **Extended Disc BASIC**
  - Powerful interactive language
  - Easy to use and understand
- **Language Extensions**
  - Enhance flexibility and capabilities
  - Provide memory management facilities
  - Direct access to memory and I/O ports
  - Extensive string operating capabilities
- **Supported by STARPLEX Disc Operating System**
  - Complete file management
  - Allocates and protects disc storage
- **Program Development Aids**
  - Minimize program development time

Product Overview

STARPLEX BASIC is an extension of the language originally developed at Dartmouth College. It provides a powerful, interactive programming language that can be used to solve a wide range of application problems. Because its instruction set resembles English statements, BASIC is easily understood and quickly learned.

Several additions to STARPLEX BASIC enhance the original language's capabilities and increase its flexibility. Among these enhancements are a complete set of data types, additional statements and functions, comprehensive data management facilities and multi-dimensional array capabilities.

STARPLEX BASIC is fully supported by the STARPLEX Disc Operating System. This allows the user to take advantage of the extensive operating system features including independent I/O and dynamically creating, accessing or deleting files. Data management features allow access to files created in any language supported by the operating system.

STARPLEX BASIC gives the programmer a wide variety of statements and commands that minimize program development time. For example, trace statements allow the execution of programs to be monitored, while edit facilities permit modifications to be made quickly and easily.

Functional Description

STARPLEX BASIC provides the user with a full range of arithmetic and relational operators, multi-dimensional arrays and mathematical functions.

STARPLEX BASIC combines features of an interpreter and a compiler. When a BASIC statement is entered from the keyboard, the program performs an immediate translation to a more compact format. This method makes more efficient use of memory than an interpreter but still permits the input source to be examined and modified.

Data Types

The following data types are supported:

- Integers (−32,768 to 32,767)
- Single Precision Floating Point (to 7 digits)
- Double Precision Floating Point (to 16 digits)
- Strings (to 255 characters)

Extensions

- Integer Division — forces arguments and quotient to integer form. It provides an operation to perform division which is eight times as fast as standard floating point.
- PEEK and POKE — allow a byte to be retrieved and stored at a specific memory location.
- INP and OUT — allow a byte to be read from or written to a specific port (not used by system).
- ERASE — allows arrays to be eliminated and their space in memory used for other purposes.
- CONSOLE — allows the console terminal to be switched to a different I/O port.

Special Features

- Error Trapping — allows the user to override system error processing and write routines to handle error recovery or provide more complete error messages.
- String Operators — enable operations on ASCII character strings similar to numeric constants. For example, strings can be compared, moved or concatonated.
- Multi-Dimensional Arrays — provide the capability to define arrays with up to ten dimensions.
- Assembly Language Subroutines — can be called from BASIC programs.

Program Development Features

- Editing Facilities — permit the user to correct, add or delete individual characters or program lines.
- MERGE Command — allows parts of two programs to be put together to form a new program.
- Direct Mode — permits immediate execution of statements without writing a program. Statements are executed as they are entered and the results displayed for later use.
- Trace Commands — cause the line number of each line in the program to be printed as it is executed. The trace function can be turned on or off by the TRON and TROFF commands.
- RENUM Command — allows program lines, branches and calls to be re-sequenced to permit insertion of new lines. The programmer may specify the increment and line number range to be renumbered.

Statement Summary

CLOSE	Finish I/O to a particular data file
DATA	Store a list of values in memory
DEF	Define a function
DIM	Allocate space for arrays
END	Terminate execution of program
ERASE	Eliminate arrays to reuse memory space
ERROR	Generate error code
FIELD	Associate a file's random buffer with a string variable
FOR . . . TO . . .	Loop control
GET	Read random file
GOSUB	Transfer to subroutine
GOTO	Unconditional branch
IF . . . GOTO . . .	Conditional branch
IF . . . THEN . . .	Conditional branch
INPUT	Read data from terminal or disc
KILL	Delete a file from the disc
LET	Assign a value to a variable
LSET	Insert string variable into random buffer
NAME	Rename file
NEXT	Loop control
ON . . . GOTO	Condition branch
ON . . . GOSUB	Conditional branch to subroutine
ONERROR GO TO	Error trapping
OPEN	Allow access to data file
OUT	Send a byte to an I/O port
POKE	Store a byte in specific location
PRINT	Print data
PRINT . . . USING	Print data using specific output format

PUT	Write random file
READ	Access data
REM	Insert remark
RESTORE	Re-read data
RESUME	Continue execution
RETURN	Return from subroutine
RSET	Insert string variable into random buffer
STOP	Stop program execution
SWAP	Exchange
WAIT	Monitor status of I/O ports

Function Summary

ABS(X)	Absolute value of X
ASC(X$)	ASCII value of first character
ATN(X)	Arctangent of X
CINT(X)	Convert X to integer
CSNG(X)	Convert X to single precision
CDBL(X)	Convert X to double precision
CHR$(I)	Return single character for ASCII I
COS(X)	Cosine of X
EXP(X)	Exponential
FIX(X)	Return truncated integer part of X
FRE(0)	Return amount of free memory space
HEX$(X)	Convert number to hexadecimal format string
INP(I)	Read byte from port I
INSTR	Search for pattern within a string
INT	Greatest integer < = X
LEFT$(X$,I)	Left justified substring
LEN(X$)	Length of string
LOG(X)	Natural log
LPOS(X)	Position of line printer head
MID$(X$,I,J)	Return specific portion of a string
OCT$(X)	String representing octal X
PEEK(I)	Read memory
POS(I)	Console cursor position
RIGHT$(X$,I)	Right justified substring
RND(X)	Random number
SGN(X)	Sign of X
SIN(X)	Sine of X
SPACE$(I)	Blank string
SPC(I)	Point blanks on terminal
SQR(X)	Square root of X
STR$(X)	Convert number to string
STRING$(I,J)	Return a string of ASCII code J
TAB(I)	Space to position I
TAN(X)	Tangent of X
USR(X)	Call user routine
VAL(X$)	Value of string
VARPTR(V)	Return address of V

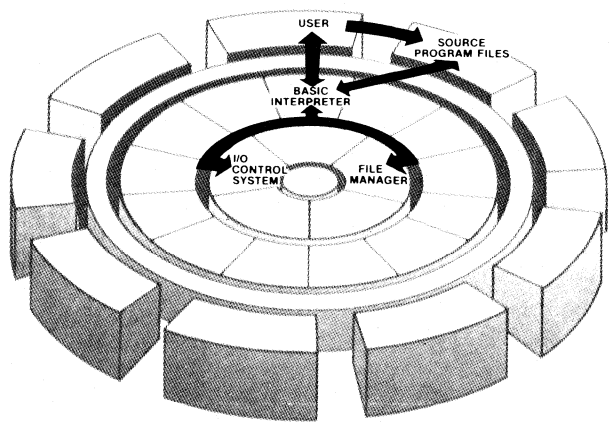
Command Summary

AUTO	Start automatic line numbering
CLEAR	Set all program variables to zero
CONT	Continue after CTRL/C, stop or error
DELETE	Delete a line or lines
EDIT	Edit a program line
LIST	List on console
LLIST	List on line printer
LOAD	Load a program from diskette
MERGE	Merge a source file from diskette into current program
NEW	Delete current program and clear all variables
NULL	Set the number of null characters to be printed at end of each line
RENUM	Re-sequence line numbers
RUN	Run the program
SAVE	Save current program as source file on diskette
SYSTEM*	Return to STARPLEX system
TROFF	Turn off trace
TRON	Turn on trace
WIDTH	Set carriage width

*Note — May be used as a program statement.

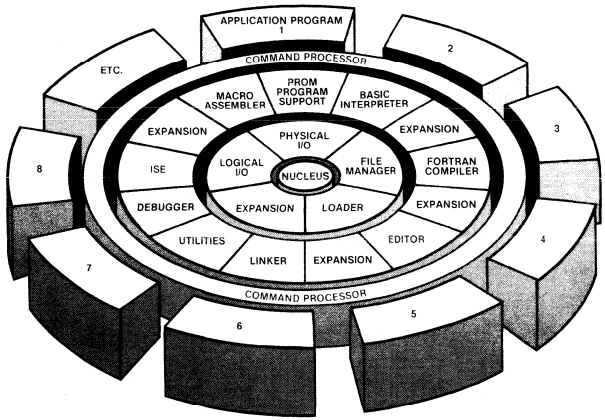
Order Information

STARPLEX™ BASIC is included with the STARPLEX Development System.



BASIC Interpreter-DOS System Diagram

STARPLEX™ FORTRAN IV



- **1966 ANSI Standard FORTRAN**
  - Programs are portable
  - Widely used language
- **Language Extensions**
  - Enhance flexibility and capabilities
  - Allow memory modification
  - Direct access to I/O ports
- **Supported by STARPLEX Disc Operating System**
  - Complete file management
  - Allocates and protects disc storage
- **User-Written I/O Drivers**
  - Non-standard devices easily interfaced
- **Extensive Library**
  - Single and Double Precision Data Types
  - Allows complex mathematical calculations

Product Overview

STARPLEX FORTRAN IV offers a widely-used, high-level language to the microcomputer user. It is a full implementation of the ANSI X3.9-1966 standard, with enhancements added to take advantage of the unique STARPLEX hardware features. Conformance to ANSI standards assures portability of existing FORTRAN programs.

Fully supported by the STARPLEX Disc Operating System, the user is provided with a complete I/O Control System and File Management facilities. These capabilities further enhance the flexibility of STARPLEX FORTRAN IV.

In addition to standard system I/O, STARPLEX FORTRAN IV allows the user to interface custom I/O drivers directly to FORTRAN programs, simplifying the task of accommodating non-standard devices.

STARPLEX FORTRAN IV offers an extensive subroutine library and supports double precision floating point data. These features enable the user to solve complex mathematical problems quickly.

Functional Description

The STARPLEX FORTRAN IV compiler is a one-pass translator which converts FORTRAN source statements into relocatable object modules. It can compile several hundred statements per minute

The compiler optimizes the generated object code in several ways:

- Common Subexpression Elimination — Subexpressions are evaluated once and the value is substituted in later occurrences.
- Peephole Optimization — In special cases, such as I = I + 1, small sections of code are replaced by faster and more compact code.
- Constant Folding — Integer-constant expressions are evaluated at compile time.
- Branch Optimizations — In arithmetic and logical IF's the number of conditional jumps is minimized.
- Error Messages — Fully descriptive error messages and listings of the generated code are additional features of the compiler.

Enhancements

- One-Byte Variables — may be used as integer quantities in arithmetic expressions, as indices in DO loops, and in arrays, as string variables. This speeds calculations, adds flexibility and reduces memory requirements.
- Mixed Mode Arithmetic — allows variables of different types to be combined in arithmetic expressions.
- Hexadecimal Constants — may be defined and used whenever integer constants are normally allowed.
- Logical Operators — manipulate bits in one-byte variables.
- EOF and ERROR Condition Transfer — may be included with READ and WRITE statements to transfer control when an error or end-of-file condition is detected.
- ENCODE/DECODE Statements — provide easy conversion from integer or real numbers into character string or vice versa.
- Random Access Input/Output — allows a record number to be specified with disc READ or WRITE statements.

Operating System Support

STARPLEX FORTRAN IV is enhanced through both operating system and utility capabilities. The interactive STARPLEX Editor allows easy modification of both programs and data. The I/O Control System provides a central facility to process all I/O commands, permitting files created in FORTRAN to be used by BASIC and Assembler language programs.

All FORTRAN IV programs and subroutines are compiled into relocatable object modules. Each can be compiled separately, generating independent object modules. Subroutines may be placed in a system library to develop a common set of subroutines. The independent object modules can then be linked to create a run-time module. If the programmer wishes to change just one module of the program, only the changed module need be recompiled.

Customized I/O Drivers

All FORTRAN Input/Output operations are table-dispatched to the driver routine for the proper Logical Unit Number. To interface a non-standard device, the user writes a driver and updates the appropriate entry in the Logical Unit Number Table. This will cause all READ and WRITE statements specifying this Logical Unit Number to use the customized driver code.

FORTRAN Subroutine Library

The standard library of subroutines supplied with STARPLEX FORTRAN IV includes:

ABS
IABS
DABS

AINT
INT
IDINT

AMOD
MOD

AMAX0
AMAX1
MAX0
MAX1
DMAX1

AMIN0
AMIN1
MIN0
MIN1
DMIN1

FLOAT

IFIX

SIGN
ISIGN
DSIGN

DIM
IDIM

SNGL

DBLE

EXP
DEXP

ALOG
DLOG

ALOG10
DLOG10

SIN
DSIN

COS
DCOS

TANH

SQRT
DSQRT

ATAN
DATAN

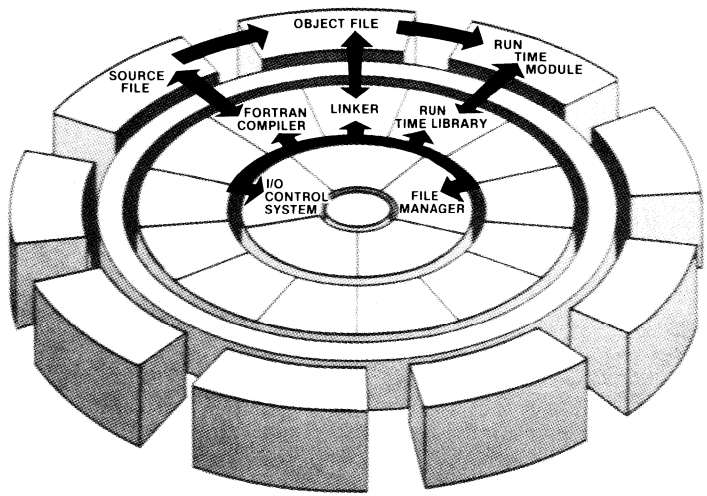
ATAN2
DTAN2

DMOD

In addition to the above list, four additional library routines — PEEK, POKE, INP and OUT are provided. PEEK and POKE allow direct access to any memory location. INP and OUT allow direct access to the I/O ports.

Comparison Table — ANSI vs STARPLEX FORTRAN IV

	FORTRAN	ANSI	STARPLEX FORTRAN
Data Type	Integer	Yes	Yes
	Real	Yes	Yes
	Double Precision	Yes	Yes
	Hollerith	Yes	Yes
	Logical (Byte)	No	Yes
Expressions	Arithmetic (+, −, *, /, **)	Yes	Yes
	Logical (NOT, AND, OR, XOR)	No	Yes
	Relational (LT, GT, LE, GE, EQ, NE)	Yes	Yes
	Mixed Mode	No	Yes
Input/Output Statements	READ/WRITE (formatted, unformatted)	Yes	Yes
	Random Access	No	Yes
	EOF and ERROR transfer	No	Yes
	ENCODE/DECODE	No	Yes
Non-executable Specifications	DIMENSION	Yes	Yes
	COMMON (blank, labeled)	Yes	Yes
	EQUIVALENCE	Yes	Yes
	EXTERNAL	Yes	Yes
	TYPE	Yes	Yes
	IMPLICIT	Yes	Yes
	DATA	Yes	Yes
	FORMAT	Yes	Yes
	BLOCK DATA	Yes	Yes
Control Statements	GO TO (unconditional & computed)	Yes	Yes
	IF (logical & arithmetic)	Yes	Yes
	CALL	Yes	Yes
	RETURN	Yes	Yes
	PAUSE	Yes	Yes
	STOP	Yes	Yes
	CONTINUE	Yes	Yes
	DO	Yes	Yes

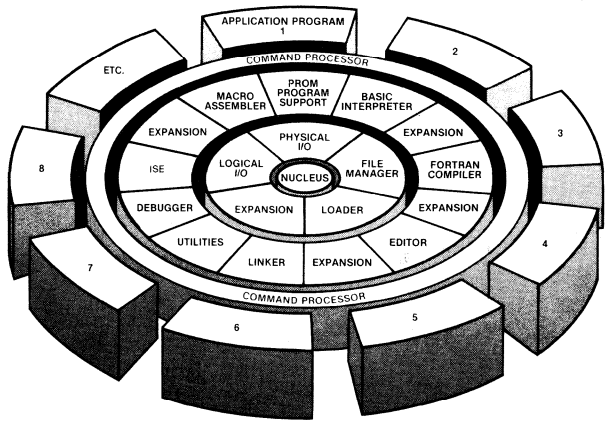


FORTRAN Compiler-DOS System Diagram

Order Information

STARPLEX™ FORTRAN IV is included with the STARPLEX Development System.

STARPLEX™ Text Editor



- **CRT Oriented Editor**
  - Text always visible
  - Minimizes errors
- **Clearly Labeled Function Keys**
  - Eliminate complex command syntax
  - Simplify training
- **Powerful Command Syntax**
  - Easily search and replace every occurrence of a specific string of characters
- **Forward and Backward Paging**
  - Provides review and correction capabilities
- **Automatic Source File Backup**
  - Protects files

Product Description

In a typical program development environment, the majority of operator interaction is with the text editor. Therefore, National has placed emphasis on the human engineering aspects of the STARPLEX Text Editor. Above all else, the editor is simple to operate and does not require constant reference to an operator's manual. The novice will find it extremely easy to use, while the expert will appreciate its simplicity and flexibility. Instructions have been replaced by labeled function keys, making it unnecessary to remember or type simple commands. Training is simplified and errors caused by miskeyed instructions are eliminated.

Unlike line-oriented editors, the STARPLEX Text Editor never requires a line number or page position to be entered. Instead, an entire page of data and the cursor are displayed. If text is to be changed, the cursor is positioned and the appropriate function key is struck. The display is constantly updated to reflect all corrections. By reviewing the text both before and after it is changed, the possibility of destroying data is minimized.

Functional Description

Text can be altered using one of four methods — type-over, insertion or deletion, and string manipulation.

Type-over allows corrections to be made by positioning the cursor at the specific character and retyping it.

Deletions and insertions of either single characters or entire lines may be made; the Editor

automatically creates or eliminates space as required.

Some commands cannot be effectively accomplished with single keystrokes. To transform the editor from single key to string oriented commands is simply a matter of depressing the STRING MODE key. The current cursor position is highlighted by reversing the video of the line in which the cursor appears. The page scrolls up, leaving a blank command line at the bottom of the screen. An asterisk (*) prompt in column one indicates that the editor is ready for a command.

Commands supported under String Mode are:

- ADD a specified block of text or file
- DELETE a range of line
- ERASETABS clear tabs
- FIND a specified character string
- HELP key list string mode commands
- INSERT COLUMN insert characters at specified column
- LIST specified range to output device
- NEXT call in next file to be edited
- OUT save intermediate EDITOR files for later re-entry
- PRINT key print contents of CRT
- REPLACE STRING replace a string of characters with another string of characters
- REPLACE COLUMN replace characters within specified columns
- STORE marks a block of data with character(s) for ADD

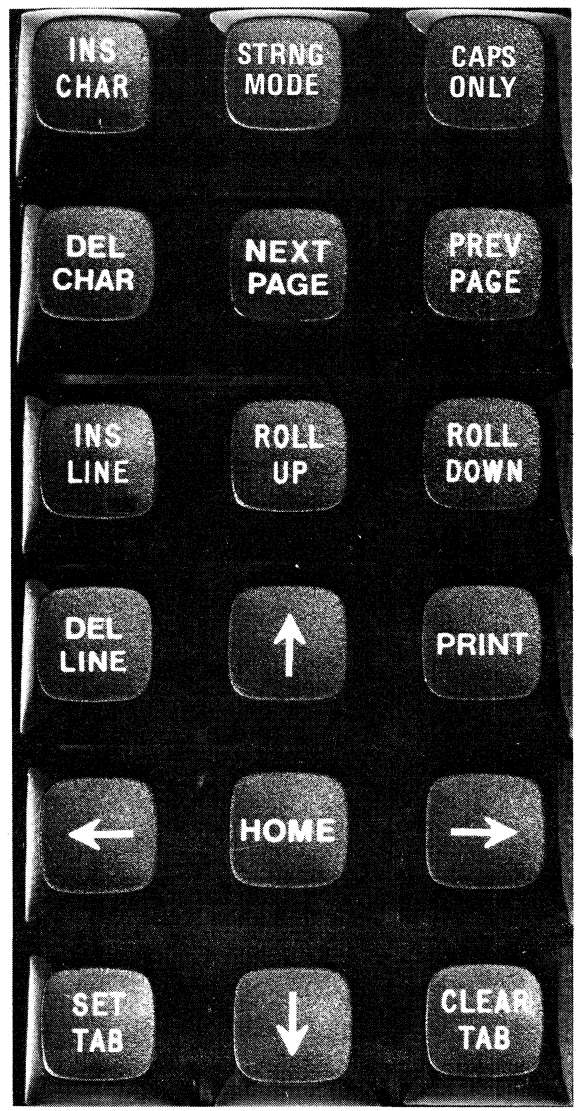
Error Handling

There are two types of errors encountered during edit operations: invalid keyboard entries which are signaled by an audible tone and ignored by the Editor, and those detected by the operating system. When the latter type of error is encountered, the Editor automatically attempts an "OUT" to save the edit session by initiating a quick exit from the Editor. The changes made during the edit session are stored in temporary files without altering the source file. To return the Editor and the file to the pre-OUT condition, the Editor is invoked by the usual means and the message "Resume previous edit session? (Y or N)" is displayed on the screen. A "Y" response restores the file to its state prior to the OUT command. An "N" response deletes the temporary files and initiates a new edit session.

The STARPLEX Editor is completely keystroke driven. If an ambiguous key is struck the Editor will signal with an audible tone and refuse to accept the implied command.

All keys are clearly labeled, and reference to an operator's manual is not necessary in order to use the STARPLEX Editor.

Editor Keypad

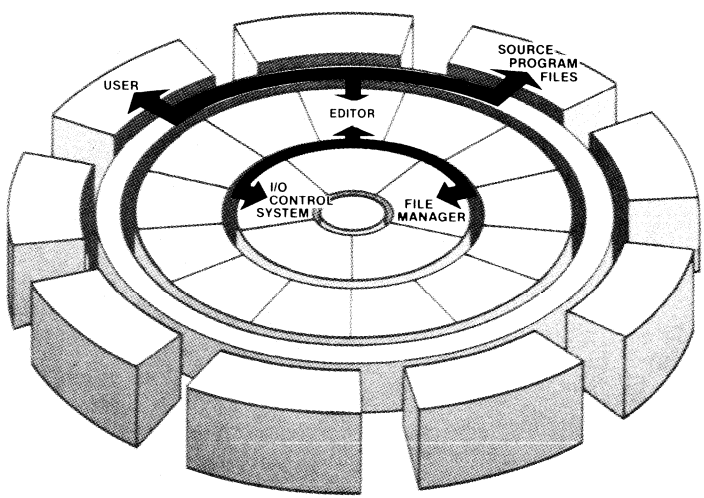


Order Information

STARPLEX™ Text Editor is included with the STARPLEX Development System.

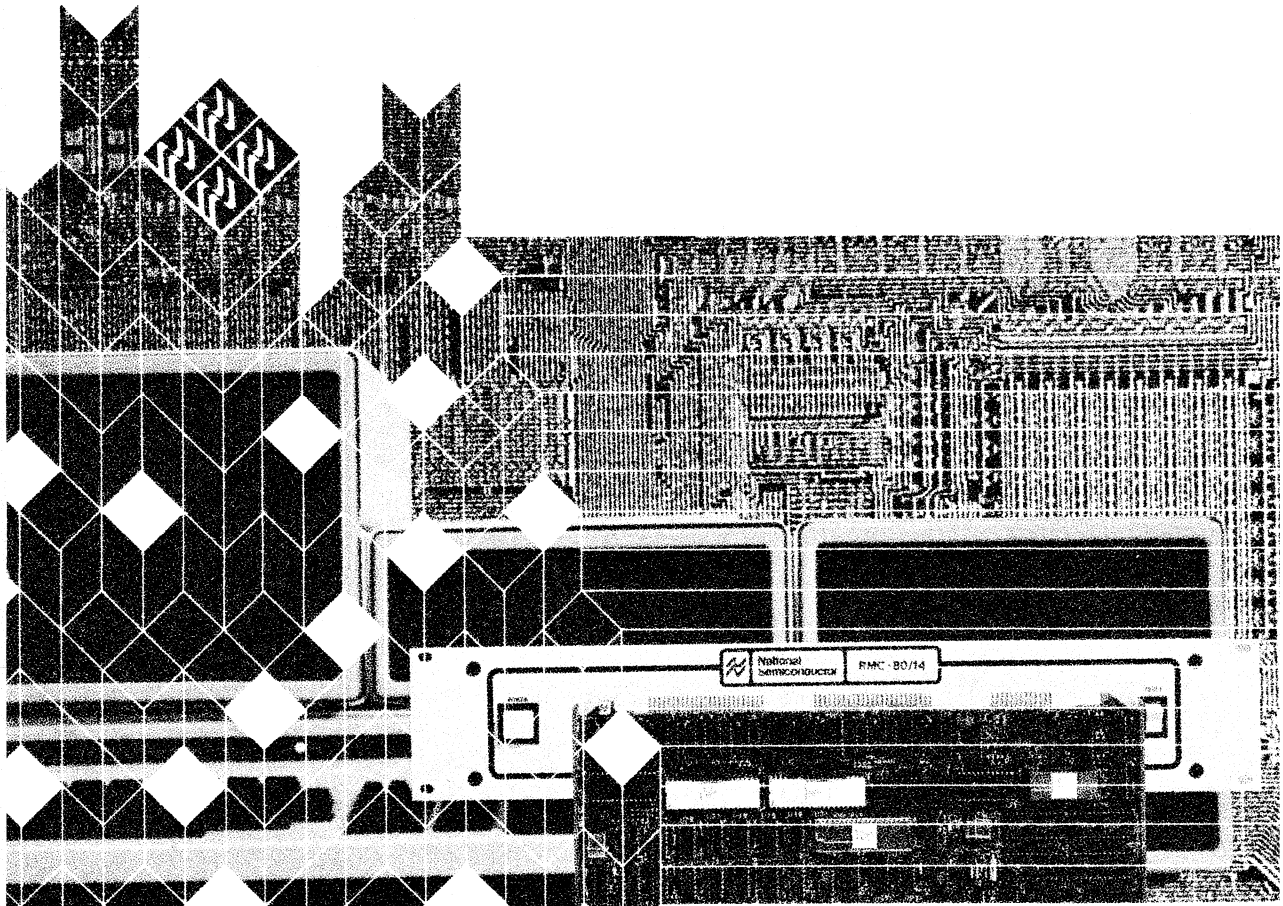
Key Description

PRINT	The CRT display is copied to the printer.
INS CHAR	The line is popped open at the cursor and the characters keyed are inserted.
INS LINE	A line of text is inserted.
DEL CHAR	The character at the cursor's position is deleted from the line.
DEL LINE	All characters from the cursor to the end of the current line are deleted.
ROLL UP	The screen is scrolled up one line.
ROLL DOWN	The screen is scrolled down one line.
STRNG MODE	Transforms TEXT EDITOR from screen oriented commands to string oriented commands.
CAPS ONLY	Sets and re-sets for all alpha upper case.
PREV PAGE	The previous page of text is displayed on the CRT.
NEXT PAGE	The next page of text is displayed on the CRT.
↑	The cursor is moved up.
↓	The cursor is moved down.
→	The cursor is moved to the right.
←	The cursor is moved to the left.
HOME	The cursor is moved to the top left position on the screen.
SET TAB	Allows the setting of user tabs
CLEAR TAB	Clears the set tab.

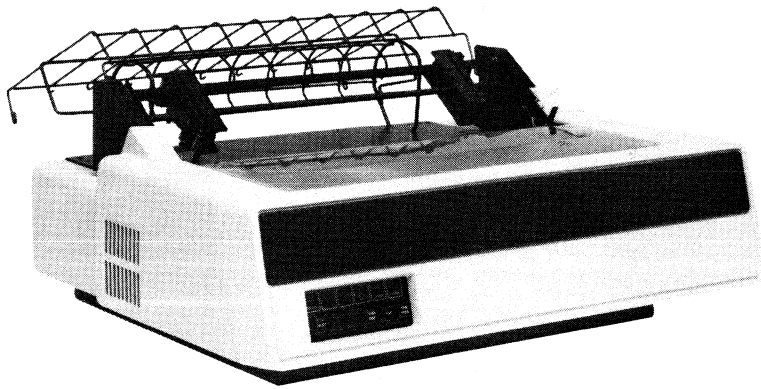


Editor-DOS System Diagram

Section 10
STARPLEX™
Options



Printers



SPM-A55 Impact Printer

The STARPLEX Development System is offered with a choice of either a thermal printer or a bi-directional impact printer.

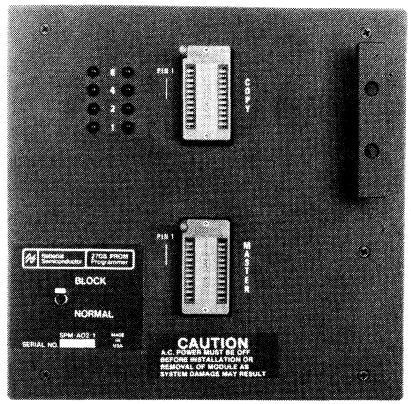
The 5 × 7 dot matrix thermal printer prints full and half size characters and operates quietly at 50 characters per second, 80 characters per line. It uses standard 8½ inch wide paper rolls which load at the top of the module. A paper advance button is conveniently located in front for ease of use.

The impact printer is logic seeking, bi-directional and operates at 132 characters per line, 120 characters per second. It has the extended ASCII 96-character set, upper and lower case, 7 × 9 dot matrix, tractor feed and uses continuous form paper from 4" to 17.3" wide with standard feed-hole edges. The impact printer allows faster throughput rates for long, multiple program listings, document files and general data processing support.

Part Number

SPM-A50 Thermal Printer
SPM-A55 Impact Printer

PROM Programmer

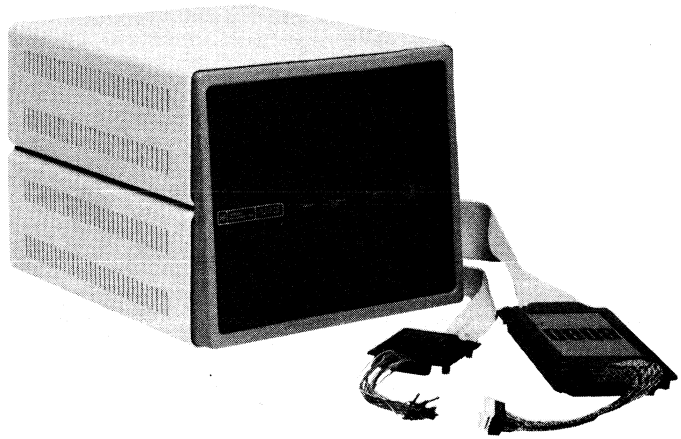


The PROM Programmer option provides a powerful and easy-to-use tool to program programmable read only memories and PALs. The PROM Programmer suppport system allows PROM code to be listed, verified and copied. When programming a PROM, the created code is written directly into the PROM mounted in the STARPLEX Development System PROM Programmer Personality Module. The source/destination for PROM data may be a PROM, diskette, memory, the video monitor or the keyboard. Personality modules are currently available for the 2708 and the 2716. The PROM programmer software package supports a variety of personality modules.

Part Number

SPM-A02	PROM Programmer Interface
SPM-A02-1	2708 Personality Modules
SPM-A02-2	2716 Personality Modules

In-System Emulator



- **A Total Emulation System**
  - Hardware
    - — CPU
    - — Breakpoint, trace, interface, memory mapping and control logic
    - — 32K byte memory
    - — Emulation processor
    - — RS232C serial port
  - Software
    - — Host resident symbolic debugger and driver software
    - — Control firmware
  - Options
    - — Target cards for 8080, 8048 family and 8070 family
    - — Cross Assemblers for 8048 family and 8070 family
- **Easy to Use**
  - Hardware
    - — 128 x 40-bit trace memory
    - — Memory mapping for 64K byte address space
    - — 35 breakpoint conditions
    - — Coast after breakpoint
    - — Breakpoint and trace load sync pulses
    - — 8-bit user status cable
    - — Microsecond timer
  - Software
    - — Symbolic debugger
    - — In-line assembler
    - — Disassembler
    - — Automatic test
    - — Full access to STARPLEX™ Development System facilities
- **Versatile**
  - Single or double microprocessor emulation
  - Variety of microprocessors supported
  - Operates with STARPLEX™ Development System

Product Overview

National Semiconductor's In-System Emulator goes beyond the single-card approach to emulation and qualifies as a genuine innovation in the development of microprocessor-based systems.

ISE is a complete stand-alone unit housing 32K bytes of user programmable memory and all the necessary logic for breakpoints, tracing and memory mapping. Microprocessor emulation is isolated on a single target card containing all the logic needed to emulate the particular microprocessor. ISE is capable of supporting two of these target cards concurrently to achieve emulation in a multiprocessor environment. ISE can support either two target cards for the same microprocessor or two different microprocessors.

There are three important advantages to a stand-alone emulation system over the emulation card approach:

Performance is the primary advantage. An emulation card must share the host system bus and memory. The card not only shares these resources; it also must compete for them in a priority scheme designed into the host system. This creates an unpredictable environment, making real-time emulation impossible.

In contrast, ISE as a stand-alone system has its own special bus designed for high speed emulation. It also has memory dedicated to the user's program, thus eliminating any conflicts and allowing real-time emulation.

Economy is another advantage of the system approach to emulation. The only difference between one emulator card and another is the microprocessor under emulation. The expensive trace memory, breakpoint logic, memory mapping logic, etc., are the same for all microprocessor emulations. The ISE module contains all the logic common to the emulation process while individual target cards are dedicated to the emulation of particular microprocessors. Each target card supported by ISE shares the total system resources, thus eliminating the unnecessary cost of supplying separate logic and memory on each emulator card.

Convenience is the most obvious advantage. The user needs to master only one software package — a single STARPLEX software driver program — which supports all features of ISE and a variety of target cards. Specific characteristics of the emulated microprocessor which must be known by the driver program (register complement, word size, status bits, etc.) are recorded in an architecture ROM located on the target card. The driver program simply reads the contents of the architecture ROM when the system is initialized. It then knows which microprocessor it is emulating and the characteristics of that microprocessor.

The ISE software package is totally integrated into the STARPLEX Development System. All of the ease-of-use concepts that set STARPLEX above other development systems are designed into the ISE system.

ISE is called with a single keystroke on the STARPLEX keyboard, as are all other STARPLEX system resources. A fill-in-the-blank menu appears on the CRT and prompts the user to select the microprocessor to be emulated. During the emulation process a portion of the CRT screen is reserved to inform the user of emulation status. This status information includes the type of microprocessor(s) selected for emulation, the state of the emulated microprocessor(s) — running, selected, present — breakpoint condition masks and whether or not breakpoints are enabled.

Should the user wish to review the full range of ISE commands available he can call for "HELP;" the "HELP" key on the STARPLEX keyboard allows the user to display information describing the ISE software functions.

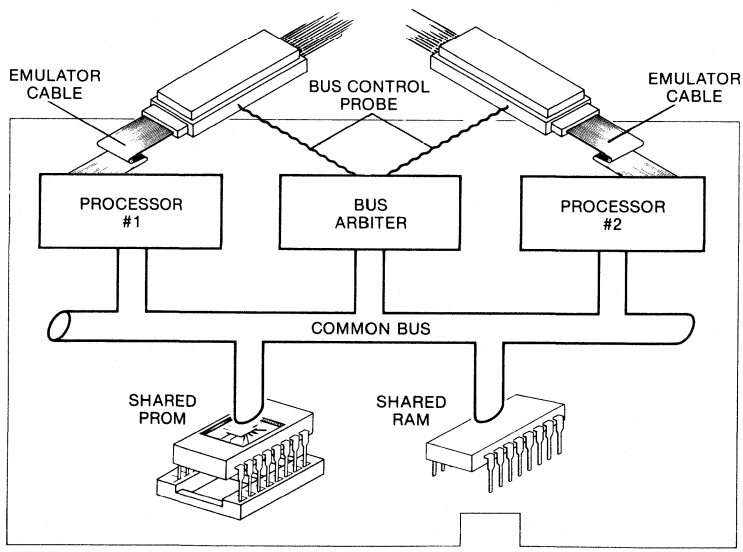


Figure 1. Application Multiprocessor System Configuration

Functional Description

Supports Various Microprocessors

The In-System Emulator is a one system solution for users who wish to prototype systems involving one or more types of microprocessors. By changing a target CPU card, ISE can be used to emulate various different microprocessors such as the 8080, 8048 family and 8070 family.

Multiprocessor Support

Many complex microprocessor-based systems use two or more microprocessors in a distributed or multiprocessor configuration. ISE will accommodate two target cards, and will support two microprocessors operating on a common on-board bus, such as National's MICROBUS™.

All memory mapping, trace and breakpoint features are available for multiprocessor emulation whenever both processors are on a common bus. When the two microprocessors are emulated in this system, breakpoints can be set on either of the microprocessors, and the trace memory will record all activities on the common bus, including which processor is on the bus during each cycle.

Multiprocessing emulation is accomplished by connecting two bus control probes from the target card cable assemblies to the application system. When attached to the user system's bus arbitration circuitry, these probes enable the user to direct ISE to dynamically monitor the target card on the common bus.

Powerful Debugging Capability

National's ISE provides all the usual features of a powerful In-System Emulator, plus many more that make it the most powerful unit available today. The usual features include: program loading from the host mass storage unit to the ISE program memory; saving programs in the ISE memory on the host system's mass storage medium; memory examination and modification; register examination and modification. Some of the additional and more powerful characteristics include:

- Real-Time Emulation of the Target Microprocessor

  Real-time emulation means that the target microprocessor is emulated in an applications system with the same hardware and software timing characteristics that the microprocessor chip will exhibit when it is plugged into the system. Real-time emulation has been designed into ISE. Some design characteristics contributing to real-time emulation are:

  — Separation of the Host Development System Function. Separating ISE from the host development system is a major contribution to real-time emulation. ISE uses a separate internal bus from the host system, thus eliminating bus access conflicts between the emulation function and the host control functions. Its internal structure is optimized for microprocessor emulation, and is not compromised by some predefined architecture. However, via the RS232C link and the driver program in the host, ISE is able to use all of the host system peripherals.

  — System Clock Selection. In the early stages of the applications system checkout, where minor timing variations are more easily tolerated, the applications system designer may choose to run the emulation using the ISE system clock. In the final checkout stages, where real-time emulation is much more critical, the designer may choose to run the emulation using the applications system clock. ISE will support either mode of operation.

  — Positioning of the Emulator Processor. Propagation delays in cables and buffers can contribute significant timing errors to the emulation process. For this reason, the emulation processor is located on a cable card only eight inches from the emulation plug to the applications system microprocessor socket. High speed buffers are used to transmit signals between the emulation processor and the applications system.

  — Emulation Processor Selection. Wherever possible an exact copy of the microprocessor being emulated is used as an emulation processor. For example, when an 8080 microprocessor is being emulated, an 8080 is used as the emulation processor. Instruction execution times and control signal timing are therefore identical to the timing that will be experienced in the final system.

- Thirty-Five Breakpoint Conditions

  Two breakpoint registers (BPC) can be defined on a 32-bit maskable word. Each breakpoint register is specified by:
  — 16 bits of address
  — 8 bits of target CPU status
  — 8 bits of user hardware status

  Each bit of the 32-bit breakpoint register mask may be specified to compare on "1" or "0," or "don't care."

  The user can then specify a breakpoint to occur when any one of the following conditions is met:
  — If BPC #1 is met
  — If BPC #2 is met
  — If BPC #1 or BPC #2 is met
  — If BPC #1 is met after BPC #2 is met
  — If BPC #2 is met after BPC #1 is met

ISE can also be told to "coast" after the breakpoint combination has been satisfied before suspending operation:

— Coast until n more BPs are encountered
— Coast until n more BPC #1s are encountered
— Coast until n more BPC #2s are encountered
— Coast until n more read/write cycles are encountered
— *Coast until n more instruction fetches are encountered
— *Coast until n more memory read/write cycles are encountered
— *Coast until n more I/O read/write cycles are encountered

Note: $0 < n < 256$.

There are five Breakpoint (BP) combinations and seven "Coast" combinations, making a total of thirty-five total combinations.

- Program Trace

  ISE maintains a constant record, in real-time, of the last 128 cycles performed by the target microprocessor. Forty bits of information are recorded for each cycle:

  — 16 bits of address
  — 8 bits of data
  — 8 bits of CPU status
  — 8 bits of user-defined status, via the 8-bit status cable

  The type of information recorded in the trace memory is selectable in four ways:

  — All read/write cycles
  — *Instruction fetches only
  — *Memory read/write cycles only
  — *I/O read/write cycles only

  ISE generates a Sync Pulse each time data is recorded in the trace memory. In addition, the user may specify that the applications program be halted after 64 words are recorded in the trace memory.

- Target Card Control Features

  The target microprocessor will be placed in an inactive state at the end of the current instruction when one of the following conditions occurs:

  — The user gives a halt-command to the given target
  — A breakpoint is encountered
  — A memory protect violation is encountered
  — Trace memory is filled with 64 words of new data, when specified
  — In single step mode

*If the target microprocessor puts out necessary status information in one form or another.

When a target is halted, the user may take any one or all of the following actions:

— Examine and change the target's internal registers
— Examine and change program memory
— Dump trace memory for examination
— Change trace specifications
— Change memory map

- Flexible Memory Mapping

  A 64K address space is available in ISE. A maximum of 32K bytes of the applications program may be mapped into ISE memory in 512-byte blocks. These blocks need not be contiguous. The memory map may be specified and altered under program control, and any segment may be write protected. In addition, data may be copied from the applications system memory.

- Microsecond Timer

  National's ISE has a 16 second timer which counts in one-microsecond increments. The user may use this timer to measure the time elapsed between any two points of his program. The two points in the program must be defined through breakpoint conditions; the clock starts counting as breakpoint condition #1 is encountered and stops when breakpoint condition #2 is encountered.

- User Status Cable

  ISE provides the user with a four foot cable carrying eight probes. The user may hook these probes anywhere in his system and treat the status of these points as part of his breakpoint word and trace word.

Convenient Software

Several tools are provided to make ISE a very convenient emulation system to use. Many of the debugging features available for software development, like symbolic debugging, are now available for system development.

- Symbolic Debugging

  Programmers use symbols to reference program and data memory when writing programs, but they are usually required to use absolute hexadecimal addresses when referencing those locations during program debug. ISE allows the designer to use those same symbols to reference program and data memory during program debug. A symbol table is generated when the program is first assembled or compiled in the host development system. That symbol table is passed to the driver program in the host system for use during the debugging operations. During debugging operations, symbols may be added or deleted, and symbol values may be redefined.

- In-Line Assembler

  A one-pass in-line assembler is provided to allow modification of object code in ISE memory or the applications system memory without having to manually convert symbolic instructions to machine language. The in-line assembler accepts program modifications in the assembly language of the target microprocessor, assembles them, and inserts them into the object program at the locations specified by the system programmer.

- Disassembler

  The disassembler examines specified segments of ISE or applications system memory, disassembles them, and displays their contents in the assembly language mnemonics of the target microprocessor. This feature eliminates many of the tedious manual steps normally involved in applications system debug.

- Automatic Testing

  The application system designer often wishes to perform a predefined sequence of tests on the system over a relatively long period of time. ISE has an automatic testing mode whereby the designer may write a sequence of test steps in a language similar to BASIC, store those tests in the memory of the host system, and initiate the test sequence. ISE will perform the tests in the specified sequence and record the results on a disc or a hard copy device of the host system. Branching and conditional branching are also permitted in the test program. This feature is especially useful for rigorous proof that all parts of the applications system are in fact working, for detecting and documenting infrequent failures, and for performing "life" tests.

  The list of predefined test sequences resides in a file created by using the ISE software or the STARPLEX™ Text Editor. Once the file is resident on the STARPLEX disc, it can be retrieved, deleted, edited, etc., by the ISE Software Package.

  The following commands allow the user to perform automatic testing functions:

DELETE	Deletes a range of lines from test program.
EXECUTE	Executes the test program.
LIST	Prints the test program to a selected device.
LOAD INFILE	Loads the specified test program fom disc.
SAVE INFILE	Saves the test program on disc.
SCRATCH	Deletes the entire test program.
END	Directive to end test program and return control to command mode.
GOTO	Unconditional branch to another statement in test program.
IF	Conditional branch to another statement in test program.
INPUT	Enables user to interact with test program at run time to specify data values.
PRINT	Prints number and string data on console.

Specifications

Memory
mappable — 32K bytes
trace — 128 x 40 bits

Power
115 VAC, 60 Hz
230 VAC, 50 Hz
345 Watts

Physical
Height — 11.31 in. (28.7 cm)
Width — 13.0 in. (33.0 cm)
Depth — 15.95 in. (40.5 cm)
Weight — 35 lbs. (15.9 kg)

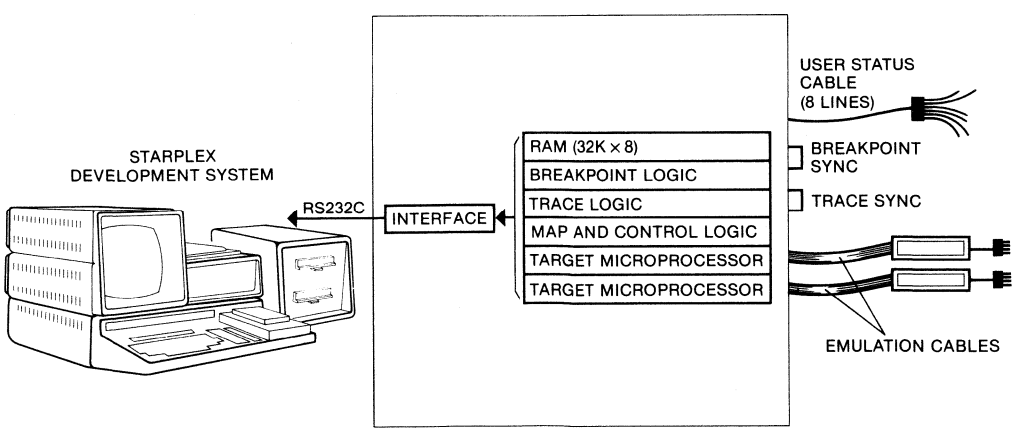


Figure 2. In-System Emulator System Configuration

Initialization and Setup Commands

SELECT or TARGET	Select target processor
LATCH	Control input from user status cable.
RESET	Set flag to reset selected target processor prior to resumption of emulation.
NORESET	Rescind RESET command.
PRINT	Select host processor's output device.
RADIX or BASE	Establish default input and display mode (binary, decimal, hexadecimal, or octal).
ARCHIVE	Save system's status on nonvolatile storage medium for later retrieval.
RESTORE	Restore system status saved by ARCHIVE command.

Emulation Commands

RUN	Continue system emulation until break condition is encountered.
STEP	Continue system emulation in single-step mode.

Memory/Register Modification and Display Commands

CHANGE	Alter contents of memory locations and registers with new data values.
DISPLAY or DUMP	Display portions of target processor memory, register or trace data.
MOVE	Transfer a region of memory into another region.
SEARCH	Search a range of memory locations for a specified value and display the location.

Breakpoint Control Commands

BREAK	Suspend emulation when specified break conditions are met in target system.
TIME	Display time between breakpoints.

Trace Control Commands

TRACE	Select target activity to be recorded into trace memory.

Memory Mapping/Demapping Control

MAP	Copy a specified memory range to or from target memory and ISE memory.
DEMAP or NOMAP	Restore a memory range previously mapped by MAP command.

Symbol Table and File Manipulation

DELETE	Delete specified symbol(s) from symbol table.
LOAD	Fetch symbol table or load file from storage medium.
SAVE	Create symbol table or load file on storage medium.

Documentation

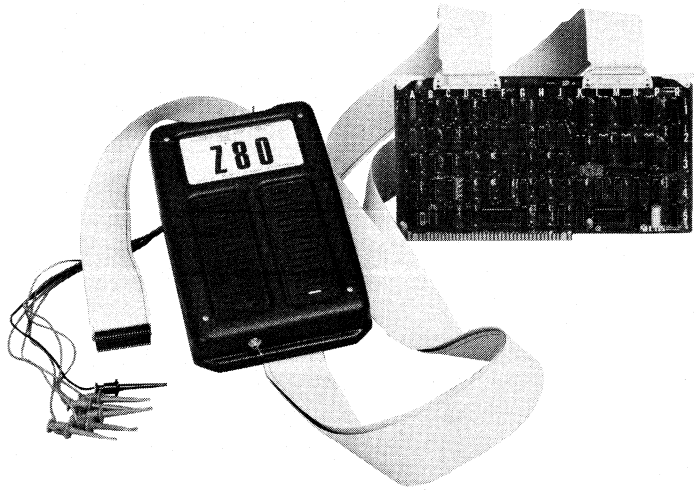
420305869-001	ISE System Reference Manual
420305653-001	8080 In-System Emulator Target Board User's Manual
420306064-001	8048 Family Cross-Assembler Software User's Manual
420306065-001	8048 In-System Emulator Target Board User's Manual
420306123-001	8070 Family Cross-Assembler (Rev A) Software User's Manual

Order Information

SPM-A08	In-System Emulator (60 Hz)
SPM-A09-1	8080 Emulator Package
SPM-A09-2	8048 Emulator Package
SPM-A09-3	8070 Emulator Package

National Semiconductor

Z-STAR™
Z-80 Development Package



- **Complete Hardware and Software for Z-80 Development on STARPLEX**
  - STARPLEX compatible target card
  - Cable module with 40-pin plug
  - Z-STAR™ emulator software
  - Z-80 cross assembler
- **Hardware Features**
  - Real-time emulation - 0.5 to 4.0 MHz
  - Flexible breakpoints allow relational breaks and BREAKREGION™, a new in-system-emulation concept
  - Memory mapping in 4K-byte blocks
  - Continuous refresh of prototype memory
  - Symbolic decoding of machine cycle and instruction trace
- **Software Features**
  - Simple, straightforward commands
  - Complete or selective reporting of emulation results
  - Symbolic trace
  - Relocatable Z-80 Macro Cross Assembler compatible with STARPLEX utilities

Product Overview

Z-STAR™ is designed for engineers who own or use a STARPLEX Development System and have the need for Z-80 development capability. Coupled with the power of STARPLEX, Z-STAR is a very powerful tool available for developing and debugging Z-80 based microprocessor products. The Z-STAR target card plugs directly into STARPLEX and interfaces easily with any Z-80 system through a flat cable terminating in a Z-80 pin-compatible plug. With this plug replacing the Z-80 device in the target system, the designer has the capability of executing the target system program in real-time while collecting up to 256 instruction cycles of real-time trace data. In addition, he can single step through his program, displaying CPU registers or memory contents at will.

Functional Description

Hardware

Z-STAR hardware consists of a printed circuit board which resides in the STARPLEX chassis and a cable assembly with external pod which interfaces to the user's prototype. Three flying leads emanating from the pod provide the user with external strobes. Another flying lead from the pod permits the user to trigger a break based on the occurrence of any TTL compatible signal generated by his prototype. An additional lead permits the counting of external events.

The Z-80 In-System Emulator implements a generalized breakpoint feature called BREAKREGION™. With BREAKREGION, the user is permitted to

define regions in memory address space as "in-bounds" or "out-of-bounds" and cause a break to occur when the program branches to an "out-of-bounds" or exits the "in-bound" region. The BREAKREGION concept facilitates hardware/software debugging by providing the user with the ability to "close-in" on a hardware fault or a software bug.

Z-STAR™ has two independent relational break registers which may be enabled or disabled. The break registers may be initialized when the emulator is in the control mode and may be re-initialized whenever a break occurs in the emulation. Also, a break in emulation may be triggered by an external pulse from the prototype system. Break conditions are formed from logical assertions of the Z-80 CPU lines.

IAK — Interrrupt Acknowledge
IOR — I/O Read
IOW — I/O Write
MRD — Read Command
MWR — Write Command
M1 — Machine Cycle
AD> — Address Greater Than
AD< — Address Less Than
AD = — Address Equal To
MEM — Memory Read or Write
IO — I/O Read or Write

Break conditions may be stated as combinations of assertions. The result is an easy-to-use and uniquely powerful debugging tool.

Software

Z-STAR software is a STARPLEX system program which provides the user with commands to define breaks and BREAKREGIONs, initiating and terminating emulation, interrogating and altering user system status, mapping STARPLEX and user memory, loading and saving user programs and printing emulation reports.

Command Summary

A	Re-executes last command typed
BK	Sets and clears breakpoints
COMM	Compare contents of a section of memory
COMF	Compares the contents of a file with the contents of memory
DO	Executes file of Z-STAR commands
EUB	Enables user breakpoint trap
FILL	Loads range of memory with any desired byte
GO	Transfers control to desired memory location or proceeds from a breakpoint
H	Hex RPN calculator
IN	Input and print a byte from any STARPLEX or user port
L	Lists breakpoints, registers, memory map, trace history or memory
LOAD	Loads user program from disk
M	Block memory move
MAP	Maps target system memory blocks into STARPLEX
SPS	Sets memory mode (user or STARPLEX)
OS	Output to STARPLEX
P	Output pulse
RESET	Resets Z-80 while at primary command level
S	Single step
SAVE	Save program
SYS	Exits to system

Z-STAR™ Z-80 Relocatable Macro Cross-Assembler

The Z-80 Cross Assembler is designed for use on the STARPLEX development system. The language syntax is compatible with both MOSTEK and ZILOG Z-80 assemblers. The assembler features both macro and conditional assembly capability. The Z-80 assembler accepts the user's program source statements and translates them into relocatable object modules. Relocatable object modules are linked together into load modules using the STARPLEX Linker command. Programs may then be executed using the Z-STAR emulator.

Z-STAR Emulator Package Specifications

Package Components —	Trace Board (1) Interface cables (2) Pod (1) Z-STAR system diskette Z-80 Cross Assembler diskette Z-80 In-System Emulator User's Manual Z-80 Cross-Assembler Manual		
Power Requirements —	5 volts ± 5% 3.5 Amps peak current		
Operating Temperature —	0 °C — 40 °C		
Physical —	Trace Board (1)	12" × 6.75"	1 lb.
	Cables (2)	5' flat ribbon shielded	
	Pod	11" × 6.75" × 2"	1.5lb
	Cable reach	7 feet	

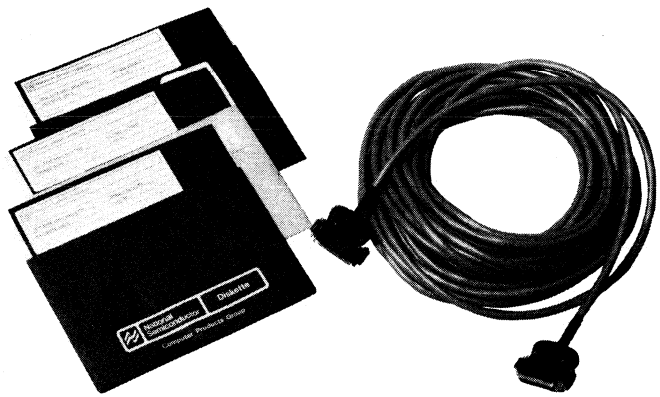
Order Information

SPM-A10	Z-STAR™ Z-80 Development Package

Z-STAR is a trade mark of National Semiconductor Corporation

BREAKREGION is a trademark of Relational Memory Systems, Inc.

STARLINK™ STARPLEX-to-MDS Comlink



- **Permits communication between STARPLEX™ and INTEL MDS230 or MDS800 systems**
- **Simple operating procedures**
- **No changes required to either system**
- **All necessary hardware and software included**

STARLINK™ is a serial link between STARPLEX and an INTEL MDS230 or 800 development system. The link provides the capability of transmitting or receiving data files over a 50-foot cable connected to the systems' RS-232 ports. Because the MDS800 does not provide an extra serial port, an I/O expansion board such as the BLC-517 is required for operation of STARLINK.

The STARLINK kit consists of the cable with connectors and three diskettes containing software necessary for operation of the link. Included are a STARPLEX diskette and two MDS diskettes (one single density and one double density). For MDS800 users a separate kit is available (Part No. AEE-A002) which includes the BLC-517 I/O expansion board.

The file transfer procedure is as follows:

- Enter the command line for the applicable MDS system into the MDS keyboard.

  For MDS230 enter — :fx:XFER MDS230 followed by a carriage return.

  For the MDS800 enter — :fx:XFER MDS800 followed by a carriage return.

  Note: x refers to the disk drive.
- Enter the name FDSx:XFER into the STARPLEX keyboard and then press the RETURN key. The STARPLEX transfer program then prompts with an asterisk "*" to indicate that commands may now be entered.
- When the asterisk appears on the screen, enter one of the appropriate commands listed below.
- The END key is depressed to exit from the Transfer program. Data is then saved and files are closed in an orderly fashion.
- The HELP key enables the user to review the list of applicable STARLINK commands. The HELP key is a feature of the STARPLEX Development System which is available to the development engineer at all stages of his program development.

Once the MDS transfer program is loaded on the MDS system, all commands to send or receive files are issued from the STARPLEX system. No other interaction is required with the MDS system. The form of commands that are issued on the STARPLEX system are as follows:

SEND<STARPLEX file>[[TO]MDS file][$Delete]

RECEIVE<STARPLEX file>[[FROM]MDS file][$Delete]

Where,

STARPLEX file	is the name of the file to be sent or received by the STARPLEX system.
TO MDS file	is the optional parameter that specifies the name of the MDS file that is sent to the MDS system from the STARPLEX system. If this filename is not specified, the STARPLEX filename is used with the device code changed to Fx: from FDSx:
FROM MDS file	is an optional parameter that specifies the name of the file that is received from the MDS system. If this filename is not specified, the STARPLEX filename is used and changed to FDSx: from Fx:
$D or $ DELETE	If the filename to be sent or received already exists, the existing file is deleted prior to transfer. If $D is specified, the file is automatically deleted. If $D is not specified, the system prompts the user for permission to delete the existing file with the following message: Delete filename? (Y or N)

All data transmissions include a checksum and retransmissions are performed automatically. Fatal systems errors are reported to the user with descriptive information so that error recovery is simplified.

Order Information

Part Number	Description
AEE-A001	STARLINK — SPX/MDS Link
AEE-A002	STARLINK — Link with BLC-517 I/O Expansion Board

Section 11
Microcomputer/ Microprocessor Training

Microcomputer/Microprocessor Training

Introduction

National Semiconductor provides training on proprietary microprocessor and microcomputer products manufactured at our facilities. The courses are available at our training facility in Santa Clara, California; or special courses tailored to your particular needs can be presented at your company site. The courses available at the training center are listed below. For further information, please contact the National Training Center at (408) 737-6453.

Micro Course
4½ Days

This course is for the Engineer, Senior Technician, or Manager who has no prior experience with program-alterable systems. It can serve as a stand-alone course for those who need only a general knowledge of microprocessors or as a "prep" course for those who need to meet the pre-requisites of the more advanced applications and programming courses.

The emphasis in this course is on basic programming techniques and the development tools used in generating applications software. Basic concepts are discussed in class and are then practiced in lab. The student must first understand what a stored program is, so the concepts behind stored programs are discussed in detail. The student is shown how he can use microprocessor "instructions" to define the function of the microprocessor at any instant in time. He is shown how a sequence of instructions can be used to define progressively complex logical functions. He is then given a simple logical function and must write a program to define the function. He must use standard development tools to make his program work. Real applications are discussed to explain the relationship between hardware and software, and to show how different types of microprocessors are needed for different real-world applications.

Prerequisites

None, however a knowledge of digital electronics, binary numbers, and Boolean algebra will be helpful.

Objectives

Upon completion of this course you will be able to:

1. Prepare a block diagram of a basic microprocessor system.
2. Write programs in machine language and assembly language.
3. Prepare source programs for assembly using a software editor.
4. Translate programs from source code to binary code using an assembler.
5. Debug and run programs on a STARPLEX™ Development System using a software debugger.

Course Outline

1. Microprocessor Introduction
   a. Basic concepts
   b. Number system

II. 8080 Microprocessor Introduction
   a. Register structure
   b. Programming convention
   c. System introduction

III. Programming Introduction
   a. Flow charts
   b. Assembly language
   c. Mnemonics, Part 1
   d. Sample programs

IV. Lab
   a. Introduction to STARPLEX
      1. Hardware
      2. Power up
      3. Debug program
   b. Load and execute sample programs

V. 8080 Hardware
   a. Chip set
   b. Timing

VI. Programming Part 2
   a. Mnemonics Part 2
   b. Sample programs
   c. Problem 1

VII. Lab —Load and Run Problem 1

VIII. Input/Output
   a. Parallel I/O
   b. Associated mnemonics
   c. Sample programs
   d. Problem 2

IX. Lab — Load and Run Problem 2

X. Interrupts
   a. Concept
   b. Associated mnemonics
   c. Programmable interrupt controller
   d. Programmable interval timer
   e. Sample programs
   f. Problem 2

XI. Lab — Load and Run Problem 3

XII. STARPLEX Development System
   a. Disk data storage
   b. Editor
   c. Assembler
   d. Linker
   e. Sample programs
   f. Problem 3

XIII. Lab
   a. Load source program using editor
   b. Assemble program
   c. Link program
   d. Run and debug program

XIV. High Level Languages
   a. Assemblers
   b. Compilers
   c. Interpreters

XV. Hardware
   a. Serial I/O
   b. Board level computer 80/20
   c. Multiprocessing
   d. STARPLEX keyboard/CRT controller
   e. Sample programs
   f. Problem 5

XVI. Lab — Load and Run Problem 5

XVII. More Hardware
   a. Direct memory access
   b. Some complex peripherals

XVIII. Lab — Problem 5 continued

XIX. Other Microprocessors and "ISE" Concept

XX. Lab — Finish Problem 5

STARPLEX™ Development System 4½ Days

This course introduces the STARPLEX Development System to the experienced engineer or programmer and prepares him to use it to its fullest capacity in developing his system software. The course describes the capabilities and operation of STARPLEX. Emphasis is on operation of the system and understanding the use of the software provided rather than on microprocessor programming. The student is shown how to use STARPLEX to prepare high level language programs, how to assemble these programs into relocatable machine code, and how to link a number of assembled programs into final binary form loading into a user's system. Expansion capabilities are discussed pointing out the usefulness of STARPLEX with new and future microprocessors. Approximately half of the course time is dedicated to lab in which the student will be provided sample programs and problems which will familiarize him with STARPLEX operation.

Prerequisites

Completion of National's Micro Course or:

1. Knowledge of a microprocessor system to a block diagram level.
2. Working knowledge of 8080 assembly language and preferably some knowledge of BASIC or FORTRAN high level languages.

Objectives

Upon completion of this course you will be able to:

1. Write and debug 8080 machine code programs on STARPLEX using the 8080 assembler or FORTRAN compiler.
2. Program EPROMs for user microprocessor systems.

Course Outline

I. Introduction
   a. Development system overview
   b. Physical description
   c. Hardware overview
   d. Software overview

II. Operation
   a. Layered executive concept
   b. Keyboard use
   c. Command interpreter
   d. Text editor
   e. Language processors
   f. System utilities
   g. File utilities

III. Programming
   a. BASIC
   b. 8080 Assembler
   c. FORTRAN compiler
   d. Access routines written in other languages

IV. Applications
   a. Chip level
   b. Board level
   c. In-system emulation
   d. Future applications

COPS Course 3 Days

This course is for the individual who has purchased, or who is evaluating, the Controller Oriented Processor System (COPS) processor and development system for use in control applications. The COPS architecture will be presented, followed by the instruction set. Example applications will be used to allow the student to practice development techniques.

Prerequisites

Completion of National's Micro Course or an understanding of basic microprocessor architecture, computer number systems and typical microprocessor control signals.

Objectives

Upon completion of this course you will be able to:

1. Write assembly language programs utilizing the COPS instruction set.
2. Develop a control system utilizing the COPS development system.
3. Determine the procedure for producing the unique mask required for a particular application.

Course Outline

I. History of COPS
   a. Product examples
   b. COPS family

II. Software
   a. BCD arithmetic
   b. Architecture
   c. Instruction set
   d. Programming

III. COPS Development System

IV. Hardware
   a. Interface
   b. Keyboard/Display
   c. A/D with COPS
   d. Device testing

V. Procedure for submitting COPS program to National Semiconductor

NSC800 Applications
4½ Days

This course provides the student with the information required to begin designing a system around the NSC800 family of microprocessor and peripheral chips. The instruction set will be presented, followed by discussions of the memory, I/O and peripheral functions available in this CMOS family. Approximately half of the class time will be spent in the laboratory developing the techniques necessary to design microprocessor applications.

Prerequisites

Completion of National's Microcourse or:

1. Knowledge of basic microprocessor architecture.
2. Understanding of binary and hexidecimal number systems.
3. Familiarity with microprocessor system control signals.

Objectives

Upon completion of this course the student will be able to:

1. Regarding the NSC800 CPU, NSC810 ROM/IO/Timer, & the NSC830 ROM/IO...
   Define all inputs and outputs and their function.
   Define the bus interface and its timing relationships.
   Develop a schematic diagram using these devices.
2. Describe the function of each NSC800 OP Code and develop simple machine language programs.

Course Outline

I. Introduction
   a. Course objectives
   b. Course outline
   c. Training aids

II. NSC800 Architecture
   a. Accumulator/Flags
   b. BC
   c. DE
   d. HL
   e. Alternate register set
   f. Index register (IX)
   g. Index register (IY)
   h. Interrupt vector register (I)
   i. Memory refresh register (R)
   j. Stack pointer
   k. Program counter
   l. Interrupt control
   m. Data/address buffers

III. NSC800 Instruction Set
   a. Loads
   b. Memory block moves
   c. Memory block searches
   d. Exchanges
   e. ALU
   f. Rotates & shifts
   g. Input & output
   h. Bit set, reset, & toggle
   i. Jumps
   j. Calls
   k. Restarts
   l. Returns
   m. Misc.

IV. Input/Output Pins
   a. Data/address
   b. Interrupt/restart
   c. Bus management
   d. Status
   e. Refresh
   f. Reset
   g. Clock
   h. Power save

V. Timing
   a. OP code fetch
   b. Memory read/write
   c. Input/output
   d. Interrupt & restart
   e. Power save

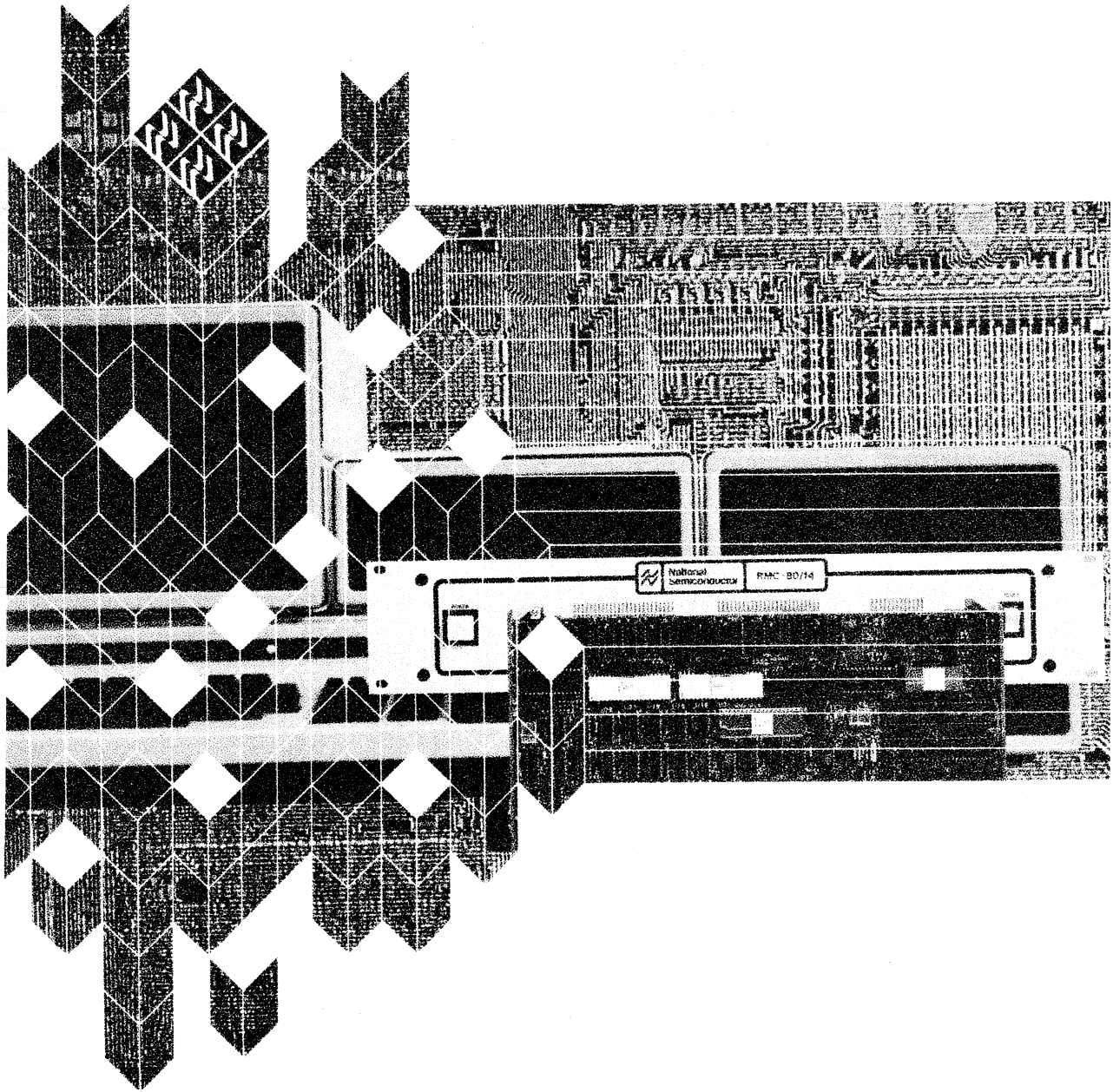
VI. NSC800 Support Chips
   a. NSC830 ROM I/O
   b. NSC810 RAM — I/O — Timer
   c. Misc. support chips

VII. Development System
   a. STARPLEX
   b. Assembler
   c. In-system emulator

VIII. System Design

IX. Review & Critique

Appendices



CPU Instructions

Appendix A

Mnemonic	Description	Execution Time (typical) Microseconds		
		BLC-80/07, 80/10, 80/11(T), 80/12(T), 80/14(T)	BLC-80/204	BLC-80/05, BLC-8715
DATA TRANSFER GROUP				
LDA	Load Accumulator Direct	6.34	6.05	6.51
LDAX B	Load Accumulator Indirect	3.42	3.26	3.51
LDAX D	Load Accumulator Indirect	3.42	3.26	3.51
LHLD	Load H and L Direct	7.81	7.44	8.02
LXI B	Load Immediate, Registers B and C	4.88	4.65	5.01
LXI D	Load Immediate, Registers D and E	4.88	4.65	5.01
LXI H	Load Immediate, Registers H and L	4.88	4.65	5.01
LXI SP	Load Immediate, Stack Pointer	4.88	4.65	5.01
MOV M,r	Move to Memory	3.42	3.26	3.51
MOV r,M	Move from Memory	3.42	3.26	3.51
MOV r1,r2	Move Registers	2.44	2.33	2.00
MVI M	Move to Memory Immediate	4.88	4.65	5.01
MVI r	Move Immediate	3.42	3.26	3.51
SHLD	Store H and L Direct	7.81	7.44	8.02
STA	Store Accumulator Direct	6.34	6.05	6.51
STAX B	Store Accumulator Indirect	3.42	3.26	3.51
STAX D	Store Accumulator Indirect	3.42	3.26	3.51
XCHG	Exchange H and L with D and E	1.95	1.86	2.00
ARITHMETIC GROUP				
ACI	Add Immediate with Carry	3.42	3.26	3.51
ADC M	Add Memory with Carry	3.42	3.26	3.51
ADC r	Add Register with Carry	1.95	1.86	2.00
ADD M	Add Memory	3.42	3.26	3.51
ADD r	Add Register	1.95	1.86	2.00
ADI	Add Immediate	3.42	3.26	3.51
DAA	Decimal Adjust Accumulator	1.95	1.86	2.00
DAD B	Add B and C to H and L	4.88	4.65	5.01
DAD D	Add D and E to H and L	4.88	4.65	5.01
DAD H	Add H and L to H and L	4.88	4.65	5.01
DAD SP	Add Stack Pointer to H and L	4.88	4.65	5.01
DCR M	Decrement Memory	4.88	4.65	5.01
DCR r	Decrement Register	2.44	2.33	2.00
DCX B	Decrement Registers B and C	2.44	2.33	3.01
DCX D	Decrement Registers D and E	2.44	2.33	3.01
DCX H	Decrement Registers H and L	2.44	2.33	3.01
DCX SP	Decrement Stack Pointer	2.44	2.33	3.01
INR M	Increment Memory	4.88	4.65	5.01
INR r	Increment Register	2.44	2.33	2.00
INX B	Increment Registers B and C	2.44	2.33	3.01
INX D	Increment Registers D and E	2.44	2.33	3.01
INX H	Increment Registers H and L	2.44	2.33	3.01
INX SP	Increment Stack Pointer	2.44	2.33	3.01
SBB M	Subtract Memory with Borrow	3.42	3.26	3.51
SBB r	Subtract Register with Borrow	1.95	1.86	2.00
SBI	Subtract Immediate with Borrow	3.42	3.26	3.51
SUB M	Subtract Memory	3.42	3.26	3.51
SUB r	Subtract Register	1.95	1.86	2.00
SUI	Subtract Immediate	3.42	3.26	3.51

CPU Instructions (continued)

Mnemonic	Description	Execution Time (typical) Microseconds		
		BLC-80/07, 80/10, 80/11(T), 80/12(T), 80/14(T)	BLC-80/204	BLC-80/05, BLC-8715
LOGICAL GROUP				
ANA M	AND Memory	3.42	3.26	3.51
ANA r	AND Register	1.95	1.86	2.00
ANI	AND Immediate	3.42	3.26	3.51
CMA	Complement Accumulator	1.95	1.86	2.00
CMC	Complement Carry	1.95	1.86	2.00
CMP M	Compare Memory	3.42	3.26	3.51
CMP r	Compare Register	1.95	1.86	2.00
CPI	Compare Immediate	3.42	3.26	3.51
ORA M	OR Memory	3.42	3.26	3.51
ORA r	OR Register	1.95	1.86	2.00
ORI	OR Immediate	3.42	3.26	3.51
RAL	Rotate Left through Carry	1.95	1.86	2.00
RAR	Rotate Right through Carry	1.95	1.86	2.00
RLC	Rotate Left	1.95	1.86	2.00
RRC	Rotate Right	1.95	1.86	2.00
STC	Set Carry	1.95	1.86	2.00
XRA M	Exclusive OR Memory	3.42	3.26	3.51
XRA r	Exclusive OR Register	1.95	1.86	2.00
XRI	Exclusive OR Immediate	3.42	3.26	3.51
BRANCH GROUP				
CALL	Call Unconditional	8.30	7.91	9.02
CC	Call on Carry	5.37/8.30	5.12/7.91	4.51/9.02
CM	Call on Minus	5.37/8.30	5.12/7.91	4.51/9.02
CNC	Call on No Carry	5.37/8.30	5.12/7.91	4.51/9.02
CNZ	Call on Not Zero	5.37/8.30	5.12/7.91	4.51/9.02
CP	Call on Positive	5.37/8.30	5.12/7.91	4.51/9.02
CPE	Call on Parity Even	5.37/8.30	5.12/7.91	4.51/9.02
CPO	Call on Parity Odd	5.37/8.30	5.12/7.91	4.51/9.02
CZ	Call on Zero	5.37/8.30	5.12/7.91	4.51/9.02
JC	Jump on Carry	4.88	4.65	3.51/5.01
JM	Jump on Minus	4.88	4.65	3.51/5.01
JMP	Jump Unconditional	4.88	4.65	5.01
JNC	Jump on No Carry	4.88	4.65	3.51/5.01
JNZ	Jump on Not Zero	4.88	4.65	3.51/5.01
JP	Jump on Positive	4.88	4.65	3.51/5.01
JPE	Jump on Parity Even	4.88	4.65	3.51/5.01
JPO	Jump on Parity Odd	4.88	4.65	3.51/5.01
JZ	Jump on Zero	4.88	4.65	3.51/5.01
PCHL	H and L to Program Counter	2.44	2.33	3.01
RC	Return on Carry	2.44/5.37	2.33/5.12	3.01/6.01
RET	Return	4.88	4.65	5.01
RM	Return on Minus	2.44/5.37	2.33/5.12	3.01/6.01
RNC	Return on No Carry	2.44/5.37	2.33/5.12	3.01/6.01
RNZ	Return on Not Zero	2.44/5.37	2.33/5.12	3.01/6.01
RP	Return on Positive	2.44/5.37	2.33/5.12	3.01/6.01
RPE	Return on Parity Even	2.44/5.37	2.33/5.12	3.01/6.01
RPO	Return on Parity Odd	2.44/5.37	2.33/5.12	3.01/6.01
RST	Restart	5.37	5.12	6.01
RZ	Return on Zero	2.44/5.37	2.33/5.12	3.01/6.01

CPU Instructions (continued)

Mnemonic	Description	Execution Time (typical) Microseconds		
		BLC-80/07, 80/10, 80/11(T), 80/12(T), 80/14(T)	BLC-80/204	BLC-80/05, BLC-8715
STACK, I/O, AND MACHINE CONTROL GROUP				
DI	Disable Interrupts	1.95	1.86	2.00
EI	Enable Interrupts	1.95	1.86	2.00
HLT	Halt	3.42	3.26	2.51
IN	Input	4.88	4.65	5.01
NOP	No Operation	1.95	1.86	2.00
OUT	Output	4.88	4.65	5.01
POP B	Pop Registers B and C off Stack	4.88	4.65	5.01
POP D	Pop Registers D and E off Stack	4.88	4.65	5.01
POP H	Pop Registers H and L off Stack	4.88	4.65	5.01
POP PSW	Pop Accumulator and Flags off Stack	4.88	4.65	5.01
PUSH B	Push Registers B and C on Stack	5.37	5.12	6.01
PUSH D	Push Registers D and E on Stack	5.37	5.12	6.01
PUSH H	Push Registers H and L on Stack	5.37	5.12	6.01
PUSH PSW	Push Accumulator and Flags on Stack	5.37	5.12	6.01
SPHL	Move H and L to Stack Pointer	2.44	2.33	3.01
XTHL	Exchange Top of Stack with H and L	8.78	8.37	8.02
INSTRUCTIONS UNIQUE TO 8085 CPU				
RIM	Read Interrupt Mask			2.00
SIM	Set Interrupt Mask			2.00

Appendix B

Parallel Input/Output Control Parameters and Modes of Operation

Port	No. of Lines	Input/Output		Unidirectional	Bidirectional	Control
		Unlatched	Latched and Strobed			
1	8	X	X	X	X	
2	8	X	X	X		
3	8	X		X		X[1]

1. Mandatory when port 1 or 2 is used in Latched & Strobed mode or port 1 is used in the bidirectional mode.

Input/Output Modes of Operation for the BLC-80/07

Port	No. of Lines	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched and Strobed	Latched	Latched and Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X[1]
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

1. Mandatory when port 1 or port 2 is used in Latched & Strobed mode or port 1 is used in the bidirectional mode.

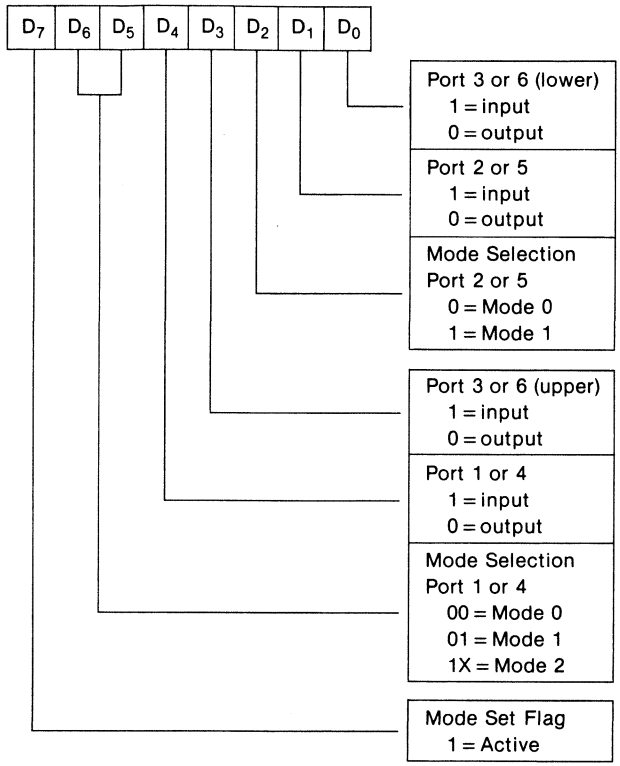
Input/Output Modes of Operation for the BLC-80/10, BLC-80/11(T), BLC-80/12(T), BLC-80/14(T), BLC-80/204, BLC-104, BLC-116, BLC-517

Port	No. of Lines	Mode of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X[1,3]
	3	X		X		X[2,3]

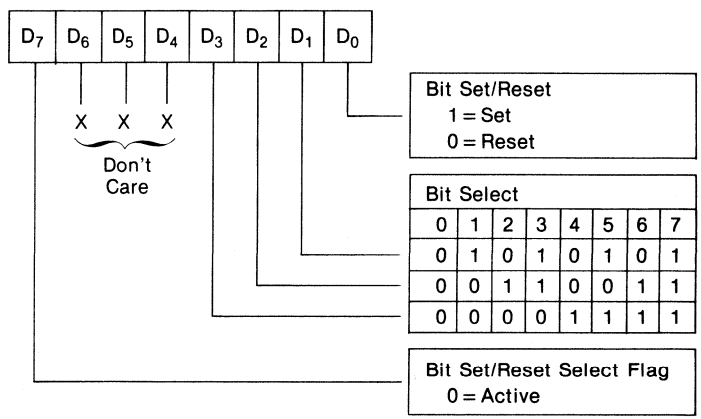
1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.
3. If both ports 1 and 2 are used in Latched & Strobed mode, they must be both input or both output ports.

Input/Output Modes of Operation for the BLC-80/05

8255/9555 Control Words

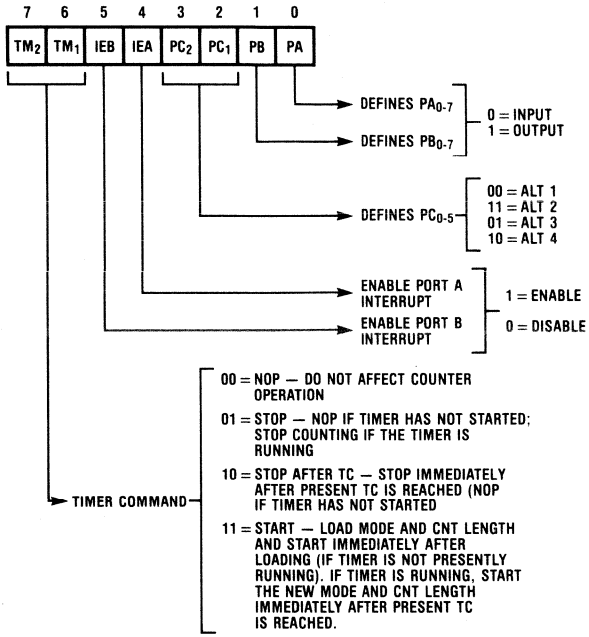


Mode Definition Control Word Format

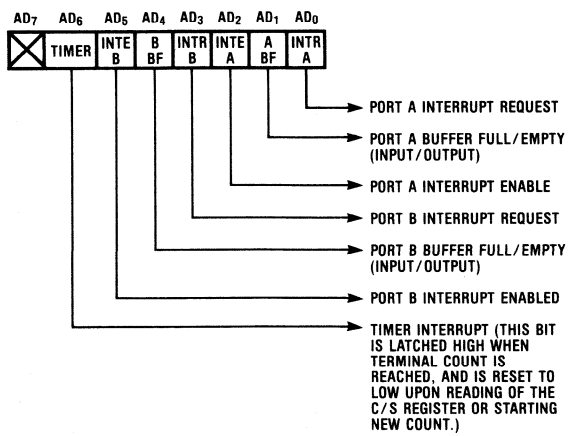


Bit Set/Reset Control Word Format

8155 Control Words



Command Register Bit Assignment



Status Register Status Word Format

NOTES

NOTES

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